ISCAS 2024

IEEE International Symposium on Circuits and Systems
May 19-22, 2024 || Singapore

Final Program

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Welcome Message from General Chairs



Dear Esteemed Colleagues and Participants,

It is with immense pleasure and excitement that we extend to you a warm welcome to the 2024 International Symposium on Circuits and Systems.

As the General Chairs, we are honored to host this prestigious gathering of minds from around the globe. Over almost one week, we will embark on a journey of intellectual exchange, collaboration, and innovation that promises to shape the future of CASS Community.

This conference represents a unique opportunity for us to come together, share our research findings, explore new ideas, and forge lasting connections within our community. Whether you are a seasoned expert or a budding scholar, your presence enriches the discourse and propels us toward new frontiers of knowledge.

Today marks a momentous occasion in the history of technology and innovation. We gather here to celebrate the 75th anniversary of the Institute of Electrical and Electronics Engineers Circuits And Systems Society, better known as IEEE CASS. As we reflect on the remarkable journey of this esteemed Society, we are reminded of its profound impact on the world.

Seventy-five years ago, a visionary group of engineers and scientists came together with a shared vision – to advance technology for the benefit of humanity. Little did they know that their humble beginnings would pave the way for a global powerhouse of innovation.

Throughout its storied history, IEEE CASS has been at the forefront of technological advancements, driving progress in fields ranging from AI, IoT, Smart cities, biomedical engineering to various applications of Circuits and Systems. It has provided a platform for collaboration, knowledge sharing, and professional development, shaping the careers of countless individuals and shaping the course of human history.

On behalf of the entire global IEEE CASS community, I extend my deepest gratitude to all those who have contributed to our success over the past seven and a half decades – our members, volunteers, partners, and supporters. It is thanks to your dedication, passion, and hard work that IEEE CASS has become the preeminent force for technological innovation that it is today.

The Organizing committee worked on a rich and very exciting program. In addition to regular sessions, special sessions, live demos and poster sessions, we added embedded workshops on emerging topics, an industrial workshop on 3D integration, a workshop on IEEE standards etc.

We also invited 5 outstanding Keynote Speakers addressing advanced topics related to CASS technical activities.

In the frame off the 75th anniversary, we are organizing a Past President Sharing Panel. They will share their experience as President of the Society and how they envision the future of the Society.

On behalf of the organizing committee, we extend our heartfelt gratitude to all our sponsors, speakers, volunteers, attendees and finally Singapore Tourism Board for their support and invaluable contributions in making this event possible.

We wish you all a fruitful and inspiring conference ahead. Let us join hands in advancing the boundaries of our field and leaving a lasting impact on society.

Welcome to ISCAS 2024

Happy CASS 75th anniversary.

Warm regards,

Pr. Amara Amara, Pr. Gwee Bah Hwee and Pr. Yong Lian
General Chairs, ISCAS 2024

Welcome Message from TPC Chairs



On behalf of the technical committee of the 2024 IEEE International Symposium on Circuits and Systems (ISCAS 2024), we welcome you to Singapore, the Perfect Symphony of Cultures.

The technical program this year consists of regular lecture and poster sessions, special sessions, keynote presentations, tutorials, live demos, embedded workshops, student design competition, and a PhD forum. The regular technical program spans the traditional as well as the emerging areas of interest to the Circuits and Systems (CAS) Society and is organized in 13 tracks. It includes 138 regular sessions (79 oral and 59 poster sessions) spread over three days. In addition to the regular sessions, we also have 34 special sessions covering various exciting CAS topics.

A total of 1497 papers from 50 different countries/regions were submitted to the conference. 1271, 202, and 24 of them went to the regular tracks, the special sessions, and the live demos, respectively. All the submitted papers were carefully peer reviewed, and the entire process was efficiently conducted online. A total of 6111 reviews were received, and each paper has an average of 4.1 independent reviews. After the rigorous review process and the deliberate discussions over the technical program committee meeting, a total of 880 high-quality papers were selected for presentations at ISCAS 2024. These include 690 papers for the regular sessions and 190 papers for the special sessions and the live demos. The acceptance rates for the regular track and the entire program are 54.29% and 58.78%, respectively.

The ISCAS 2024 technical program starts on Sunday with cutting-edge tutorials as part of the ISCAS tradition. This year, we have 3 full-day and 10 half-day tutorials offered by leading research experts, and the topics cover a wide spectrum in the CAS field. The keynote presentations are always the highlight of the conference. Just after the opening ceremony on Monday, we have two keynotes in the morning and another after lunch. We also have two more keynotes in the morning on Tuesday. Namely, ISCAS 2024 features five high-profile keynote speeches from renowned researchers worldwide. In the order of their presentations, they are Prof. Aaron Thean (National University of Singapore), Prof. Gert Cauwenberghs (University of California San Diego), Prof. Sandro Carrara (Swiss Federal Institute of Technology Lausanne), Dr. Hemanth Jagannathan (IBM Research, USA), and Prof. Chi K. Michael Tse (City University of Hong Kong). To encourage more interactions among the experts and the attendees from all over the world, we have organized many embedded workshops throughout the conference this year; the Climate Change Workshop, the Technology for the Elderly (GeronCAS) Workshop, the Information Security Workshop, the Autonomous Mobility CAS (AutoCAS) Workshop, the CASS Standard Association Workshop, and the 3D Integration and Advanced Packaging Workshop.

We want to thank the people who have contributed to making this technical program a high-quality one. Our thanks first go to the 28 Chairs and Co-Chairs of the 13 Tracks, the 461 Review Committee Members, and the 2793 reviewers for their great efforts in coordinating and conducting the paper reviews. We are especially thankful for the Special Sessions Chairs, Prof. Mohamad Sawan, Prof. Volkan Kursun, and Prof. Nathalie Deltimple, who have managed to come up with an exciting program for the special sessions. Our appreciation also goes to the Tutorial Chairs, Prof. Massimo Alioto, Prof. Elena Blokhina, and Prof. Francois Rivet, for putting together an exciting set of topics and speakers. We would like to thank the great support of the Keynote Chairs Prof. Andrei Vladimirescu and Prof. Jan Rabaey, the Cross-Society Special Session Chair Prof. Xinmiao Zhang, the Embedded Workshop Chair Prof. Fakhrul Zaman Rokhani, and the Live Demonstrations Chairs Prof. Chao Wang and Prof. Deruo Cheng.

A conference cannot be successful without a strong logistic support. The entire review process for ISCAS 2024 was carried out using a professional online, web-based review system. For this, we would like to thank Tom Wehner from Epapers for his timely assistance and experience sharing. We are also indebted to the Singapore local organizing committee members, who have coordinated all technical program-related matters in an orderly and efficient manner. Finally, we would like to thank all the authors for their excellent contributions, which led to a high-quality and exciting technical program.

In closing, we wish all participants a stimulating and fruitful time at the conference and a pleasant stay in the Lion City.

Yoshifumi Nishio, Victor Grimblatt, and Nam Ling
TPC Chairs, ISCAS 2024

IEEE ISCAS 2024 Organizing Committee

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Jan Rabaey, University of California, Berkeley, USA

Special Session Chairs

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Cross-Society Special Session Chair

Xinmiao Zhang, The Ohio State University, USA

Tutorial Chairs

Massimo Alioto, National University of Singapore, Singapore
Elena Blokhina, University College Dublin, Ireland
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About the IEEE Circuits and Systems Society

The IEEE Circuits and Systems Society (CASS) is the leading organization that promotes the advancement of the theory, analysis, design, tools, and implementation of circuits and systems. The field spans their theoretical foundations, applications, and architectures, as well as circuits and systems implementation of algorithms for signal and information processing.

The Society brings engineers, researchers, scientists and others involved in circuits and systems applications access to the industry's most essential technical information, networking opportunities, career development tools and many other exclusive benefits.

Local members with similar technical interests engage in professional exchange through the Society's 10 regional chapters in the United States, Canada, Europe, the Middle East, Africa, Latin America, Asia, Australia and the Pacific.

Objective
The purposes of the Society are scientific, literary and educational in character, directed toward the advancement of the theory and practice of electrical, electronics, and allied branches of engineering or the related arts and science, in order to increase the professional standing of the Members and Affiliates.

The Society shall aid in promoting close cooperation and exchange of technical information among its Members and Affiliates, and as means to these ends shall hold public meetings for the reading and discussion of periodical and special works of literature, science and art pertaining thereto, the initiation and development of engineering standards, and any other activities necessary, suitable and proper for the fulfillment of these objectives. Through its Committees the Society shall study and provide for the needs of its Members and Affiliates.

CASS Field of Interest
The theory, analysis, design, tools, and implementation of circuits and systems. The field spans their theoretical foundations, applications, and architectures, as well as circuits and systems implementation of algorithms for signal and information processing.

Our Mission
To foster technological innovation and excellence in fundamentals, emerging directions and application of circuits and systems for the benefit of humanity through an interdisciplinary community.

Our Vision
To advance and promote Circuits and Systems knowledge framed in interdisciplinarity to be essential to the global and diverse technical community and be universally recognized for providing and leading solutions to the United Nations' Sustainable Development Goals.

IEEE Circuits and Systems Society Leadership Team

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Woogeun Rhee, Tsinghua University

CASS 75th Anniversary

Celebrating 75 years of innovation, the IEEE Circuits and Systems Society (CASS) proudly presents its commemorative logo. Infused with the Society's legacy, the number '75' integrates electronic circuit patterns, symbolizing the intricate work and progress in the field of circuits and systems. The dynamic swoop around the 'CAS' acronym reflects a modern, inclusive, and forward-moving organization. This logo stands as a beacon of the Society's dedication to advancing technology for the betterment of humanity, marking its historic 75th anniversary with a nod to its foundational past and a bright gaze toward the future of electronics.

In the lead-up to the IEEE CASS 75th anniversary, a series of pre-event activities are set to build excitement and engagement among members worldwide. Starting on April 5th, 2024, and running until May 21st, 2024, Celebrations @ Chapter & Student Branch Chapters will allow members to participate in the festivities remotely, culminating in a virtual event on May 21st. In addition to these celebrations, a 75th Anniversary Digital badge will be introduced to commemorate this milestone. Participants are also invited to engage in a Photo & Video contest that showcases their creativity and experiences within the Society, along with a Trivia event that will test their knowledge of CASS's rich history.

To amplify the 75th anniversary celebrations, the IEEE CASS has developed a comprehensive Promotion Toolkit that includes a variety of branded materials. This toolkit features the specially designed 75th Anniversary logo and a unique mascot that embodies the spirit of the Society. Members can enhance their online presence with Digital backgrounds for virtual meetings, and promote the event locally with a 75th Anniversary poster and digital banners. These tools are designed to foster a unified celebratory atmosphere across all chapters and enhance the visibility of the Society’s landmark anniversary.

The celebration will reach its peak at the IEEE International Symposium on Circuits and Systems (ISCAS), where a dedicated 75th Anniversary lounge will be set up from Leo 2 to 4. The event will feature the launch of the 2nd Edition of "A Short History of Circuits and Systems" Book, enriching members' understanding of the Society’s impact on the technological world. Attendees can capture memories at a Photo Booth equipped with a 75th Anniversary Photo Mosaic, and notable contributions will be recognized during the IEEE CASS Award ceremony, which includes categories like Best Contribution and Best Mascot. The festivities will also include a ceremonial cake cutting—with a twist on tradition, featuring cupcakes—and a special anniversary song performed by a band, adding a musical flair to the celebrations.

Organized by: Yongfu Li, Fakhrul Zaman Rokhani, Yoko Uwate, Fidel Makatia, Hanho Lee, Brianna Orr, Lacey Glasscock, Molly Brackin, Myung Hoon Sunwoo

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Keynote Speakers

Monday, May 20th | 09:00 – 10:00
Title: Towards Chips that Rewire Themselves? …How Novel Material-System Co-Design can enable them
Speaker: Aaron Thean, Deputy President (Academic Affairs) and Provost, National University of Singapore, Singapore

Ultra-low energy and area-efficient electronic systems are required to enable untethered computing at the edge of IoT. To realize self-learning edge-AI systems, conventional solely software-driven deep-learning neural networks becomes a major roadblock due the excessive energy expense of training. Hence, fundamental hardware change is likely needed. In this talk, we review our recent material innovations (E.g. Ferroelectric oxides and 2D Material) and we show how close coupling with new micro-architecture innovations (E.g. New memory physical layout and Monolithic 3D IC) may significantly accelerate in-memory computation. We explore wafer-level solution-processed CMOS-compatible use of 2D Material (MoS_2/WSe_2) to enable high-endurance memristors that can have properties superior to conventional oxide RRAMs. We discuss the use and enabling of multi-gated HZO-based low-thermal-budget ferroelectric oxide memtransistors for new reconfigurable non-volatile logic and interconnect. In co-operation with specific system-level innovations, we review material-system co-design in data encoding for deep convolution neural network. We show through material-device-aware data encoding, error correction, and novel physical memory layout (staggered + Manhattan arrays), that aim to simplify in-memory data process, one can significantly manage variabilities while accelerating convolution deep neural network operations and offer substantial low-energy opportunities towards reconfigurable Edge-AI systems.

Biography:
Aaron Thean is a Professor of Electrical and Computer Engineering at the National University of Singapore (NUS). He currently the Deputy President (Academic Affairs) and Provost at NUS. In addition, he holds several technical leadership responsibilities at the University; which includes Director of SHINE research center on Next-Generation Hybrid Electronics research, and the founding Director of the Applied Materials-NUS Corporate Laboratory on Advanced Materials Research. Prior to NUS, Aaron Thean was the Vice President of Logic Technologies at IMEC. Working with Semiconductor Industry leaders like Intel, TSMC, Samsung, Globalfoundries, Apple, and Sony, he directed the research and development of next-generation semiconductor technologies and emerging nano-device architectures. Prior to joining IMEC in 2011, he was with Qualcomm's CDMA technologies in San Diego, California. Aaron and his group worked on Qualcomm's 20nm and 16nm mobile System-On-Chip technologies. From 2007 to 2009, Aaron was with IBM, where he developed the 28-nm and 32-nm low-power bulk CMOS technology at IBM East Fishkill, New York. Before IBM, Aaron was with Freescale Semiconductor (and Motorola) where he led research on many novel devices. Aaron graduated from University of Illinois at Champaign-Urbana, USA, where he received his B.Sc. (Highest Honors), M.Sc., and Ph.D. degrees in Electrical Engineering (Edmund J. James Scholar). He has published over 300 technical papers and holds more than 50 US patents.

Monday, May 20th | 10:00 – 11:00
Title: Moore with Less: Ultra-Low Energy Neuromorphic Circuits and Systems for Large-Scale Distributed AI
Speaker: Gert Cauwenberghs, Professor, Co-Director of the Institute for Neural Computation, University of California San Diego, USA

The rapidly increasing volume of computational power needed to train and run ever more sophisticated models in artificial intelligence, driven by an insatiable appetite for access to information about anything anywhere and anytime, is consuming massive amounts of energy depleting the earth's resources and aggravating climate change at an alarming rate. Inspired by the efficiency, efficacy, and resilience of natural intelligence in biological information processing systems, a principled approach to neuromorphic engineering design offers sustainable alternatives for ultra-low energy cognitive computing in massively parallel distributed architecture, permitting continued advances in Moore's law scaling of semiconductor technology as shrinking device dimensions approach physical limits where individual operational reliability is no longer warranted. System-level accuracy and efficiency emerge from the robust adaptive collective dynamics of large assemblies of imprecise individual nanoscale elements which, like neurons and synapses in the central nervous system, operate near fundamental thermodynamic limits of noise-energy efficiency. Examples include a fully silicon integrated memristive computein-memory chip to combine at once superior energy efficiency and near-full digital equivalent accuracy supporting a versatile range of model architectures for reconfigurable and heterogeneous AI on the edge, and a chargedomain compute-in-memory array with resonant adiabatic energy recovery consuming less than one femtojoule of energy per multiply-accumulate synaptic operation approaching nominal efficiency of synaptic transmission in the mammalian brain.

Biography:
Gert Cauwenberghs is Professor of Bioengineering and Co-Director of the Institute for Neural Computation at UC San Diego, La Jolla CA. His research focuses on micropower integrated biomedical circuits, neuron-silicon and brain-machine interfaces, neuromorphic engineering, and adaptive intelligent systems. He is a Fellow of IEEE and the American Institute for Medical and Biological Engineering (AIMBE). He served IEEE in a variety of roles including as Distinguished Lecturer of the IEEE Circuits and Systems Society, as VP of Technical Activities on the Executive Committee of the IEEE Engineering in Medicine and Biology Society, on the Steering Committee of IEEE Brain, and as Editor-in-Chief of the IEEE Transactions on Biomedical Circuits and Systems.

Monday, May 20th | 14:00 – 15:00
Title: More Sustainable Bio/CMOS Interfaces for Remote Human Health
Speaker: Sandro Carrara, Professor, Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland

The emerging era of wearable devices will lead to a real development of distributed diagnostics by through several personal devices that allow remote monitoring and actuation for better human health. This typically means remote monitoring and actuation of human vital signs, including at molecular level as required by the modern concept of precision medicine. To that aim, new and definitely more reliable and specific tools need to be developed in terms of portable, wearable, and also implantable devices. Therefore, we will discuss in this keynote the constrain of the required advanced approaches to fruitfully address such request for new personal technology for health. Such new technology is required to be so minimally invasive to became almost ¨hidden¨ or ¨forgot¨ by the end user, including electronics dusts (see, for example, the concept of neural dust). Furthermore, many different new features need to be included in these new devices, including while not limited to edge-computing and in-memory computing. So, the present keynote will present a series of recent advancements in the field of portable, wearable, and also implantable Bio/CMOS interfaces, with applications to diseases monitoring in precision medicine and prosthetic devices, with capability of local computation. On the other hand, one of the present challenges of the worldwide humanity is designing more sustainable technologies in all the field of application. Therefore, this keynote will also address this issue by showing a series of new advancements in developing more sustainable approaches for Bio/CMOS interfaces.

Biography:
Sandro Carrara is an IEEE Fellow of the Circuits and Systems Society. He also is the recipient of the IEEE Sensors Council Technical Achievement Award. He is Professor at the EPFL in Lausanne (Switzerland), and head of the Bio/CMOS interfaces laboratory. He is a former professor at the Universities of Genoa and Bologna (Italy). He holds a PhD in Biochemistry and Biophysics, a Master degree in Physics, and a diploma in Electronics. His scientific interests are on electrical phenomena of nano-bio-structured films, and include CMOS design of biochips based on proteins and DNA. Along his carrier, he published 7 books, one as author in 2013 (2nd Edition in 2024) with Springer/NATURE on Bio/CMOS interfaces, and a Handbook of Bioelectronics with Cambridge University Press. He has now 400 publications and 17 patents. He is an Associate Editor of IEEE Transactions on Biomedical Circuits and Systems. He is former Editor-in-Chief of the IEEE Sensors Journal, and founder and former Editor-in-Chief of the journal BioNanoScience by Springer. He was a member of the Board of Governors (BoG) of the IEEE CAS Society, and currently is Vice President Publications for the IEEE Sensors Council. He has been appointed IEEE Distinguished Lecturer of the CAS Society in 2012. His work received several other international recognitions as best-cited papers and best conference papers. in 2014, he has been the General Chairman of the Conference IEEE BioCAS, the premier conference in the field of circuits and systems for biomedical applications.

Tuesday, May 21st | 10:30 – 11:30
Title: Semiconductor Innovations to Continue and Go Beyond Moore's Law in the Era of AI
Speaker: Hemanth Jagannathan, IBM Distinguished Engineer, Chiplet & Advanced Packaging Technology, IBM Research, USA

Artificial intelligence is transforming our world and the demand for computing capability is increasing at an unprecedented pace. We will talk about semiconductor technology innovations in logic, memory, and advanced packaging to meet this ever-growing demand in the era of AI.

Biography:
Hemanth Jagannathan is a Distinguished Engineer at IBM. He has driven key technical advancements over several generations of semiconductor technologies ranging from planar, FinFET to Nanosheet and beyond nanosheet device architectures. Hemanth is currently the technical executive responsible for Chiplet and Advanced Packaging Technology at IBM Research. He received his Ph.D. in Electrical Engineering from Stanford University and began his technical career at IBM working on high-k metal gate technology. He drove multiple innovations on novel gate stack materials and processes that are being used to this day in advanced CMOS logic technologies. Hemanth also led the advanced semiconductor FEOL process technology team and was responsible in defining the comprehensive semiconductor process strategy for beyond planar, FinFET, Nanosheet and future device architectures. He was the Hardware Technologist who spearheaded the innovations for the Vertical-Transport Nanosheet Field Effect Transistor (VTFET) program at IBM.

Hemanth serves as an IBM representative in multiple academic engagements across the US. He is the executive director for the SUNY-IBM Artificial Intelligence Collaborative Research Alliance where he oversees joint AI research ranging from hardware, algorithms to software and applications. Hemanth is the recipient of multiple IBM Outstanding Technical Achievement Awards and Research Division Awards for his technical accomplishments. He is a senior member at IEEE and has authored/co-authored over 100 technical publications and holds over 200 patents in the semiconductor area.

Tuesday, May 21st | 11:30 – 12:30
Title: The Evolving Power Grid Towards a Greener Future
Speaker: Michael Tse, Chair Professor of Electrical Engineering and Associate Vice President at City University of Hong Kong, Hong Kong

As prompted by the increasing use of renewable sources and the quest for higher performance in the control of power conversion, the use of power electronics in generation and distribution systems has increased significantly in recent years,. Interactions of power electronics systems and conventional synchronous machines' dynamics would inevitably cause stability and robustness concerns, which can be understood from the conventional control viewpoint and the coupling effects among interacting dynamical systems of varying stability margins (or transient performances). In this talk, we discuss the various circuits and systems problems of power electronics penetration into power grids and the implications on the continuous evolution of the power grids.

Biography:
C K Michael Tse received the BEng (Hons) degree in electrical engineering and the PhD degree from the University of Melbourne, Australia. He is currently Associate Vice President, Director of Academy of Innovation, and Chair Professor of Electrical Engineering with City University of Hong Kong. His research interests include power electronics, nonlinear systems, and complex network applications. Prof. Tse was the recipient of a number of research and industry awards, including the IEEE CASS Charles A. Desoer Technical Achievement Award in 2022, Prize Paper Awards by IEEE Transactions on Power Electronics in 2001, 2015, 2017, 2021 and 2022, four Gold Medals and Grand Prizes at the international invention exhibitions, and a number of recognitions by the academic and research communities, including honorary professorship by several Chinese, Canadian and Australian universities. He was the Editorin-Chief for the IEEE Transactions on Circuits and Systems II from 2016 to 2019 and IEEE Circuits and Systems Magazine from 2012 to 2015, and on the editorial boards of a few other IEEE journals. He was elected as an IEEE Fellow in 2005.

Tutorials

1. Full Day: Mixed-Signal RF Transmitters

Instructor(s):
- David J. Allstot (Distinguished Special Professor, Carnegie Mellon University, USA)
- Vanessa Chen (Assistant professor, Carnegie Mellon University, USA)
- Jeffrey S. Walling (Associate Professor, Virginia Tech, Blacksburg, VA, USA)

Abstract/Information:
For nearly 100 years, RF transmitter frontends have been dominated by linear analog mixing architectures. Meanwhile, in the era of integration, the transistor has been optimized for small area and low resistance switching. Hence, radio architectures that exploit more the switching performance of the transistor should be considered. Digital power amplifiers operating in resistance-mode as programmable inverse-class-D amplifiers and in the voltage-mode as class-D amplifiers (e.g., Switched-Capacitor Power Amplifiers (SCPAs)) have been extensively proposed and investigated recently, as a potential solution to the aforementioned architectural transformation in wireless transmitters. However, these transmitters do not have myriad textbooks detailing their operation that are available for more traditional analog based transmitters. These switched-mode transmitters require operation from the digital baseband to the antenna interface and hence require strong multi-disciplinary skills from digital signal processing to RF impedance matching. It is anticipated that such mixed-signal transceivers will only become more popular in the era of 6G, where support for multi-band and multi-mode operation is critical, and where a shift back to centimeter wave spectrum will again make mixed-signal transmitters more competitive. Hence, a tutorial that focuses not only on operation principles, but also on simulation and design methodology of mixed-signal transmitters is called for. In the proposed tutorial, the speakers will focus on the switched-capacitor power amplifier, however, other mixed-signal transmitters will also be covered and the attendee to the tutorial will learn the basics required to begin their own designs and also learn of case studies detailing recent, specific implementations.

2. Full Day: Advanced Biomedical Imaging Technologies: Circuit Design and Techniques

Instructor(s):
- Yuanjin Zheng (Professor, Nanyang Technological University, Singapore)
- Yongfu Li (Associate Professor, Shanghai Jiao Tong University, China)
- Jian Zhao (Associate Professor, Shanghai Jiao Tong University, China)
- Ka-Meng Lei (Assistant Professor, University of Macau)

Abstract/Information:
This tutorial series provides a comprehensive exploration of four cutting-edge biomedical imaging technologies: radar and ultrasound, electrical impedance tomography, functional near-infrared spectroscopy, and magnetic resonance imaging. Delving into the heart of circuit design and imaging techniques, participants will gain invaluable expertise in harnessing these technologies for practical applications in healthcare and diagnostics. By the end of the tutorials, attendees will be equipped to drive innovation in the field, leading the way towards enhanced medical imaging and superior patient care.

3. Full Day: Integrated Devices, Circuits and Systems for Quantum Computing

Instructor(s):
- Andreas Fuhrer Janett (Research Staff Member, IBM Research Europe, Zurich, Switzerland)
- Christian Enz (Professor, EPFL, Switzerland)
- Andrei Vladimirescu (Professor, University California Berkeley, CA, USA)
- Fabio Sebastiano (Associate Professor, TUDelft, The Netherlands)
- Edoardo Charbon (Professor, EPFL, Switzerland)
- Joseph Bardin (Professor, UMass/Google, MA, USA)
- Sorin Voinigescu (Professor, University of Toronto, Ontario, Canada)
- Domenico Zito (Professor, AGH University of Science and Technology, Krakow, Poland)

Abstract/Information:
Quantum Computing is a most far-reaching and challenging emerging technology. The control and readout of the fundamental properties of matter at atomic scale, such as spin, superposition, entanglement and decoherence will radically transform the future technology developments and science discoveries. This tutorial addresses the fundamentals and case studies of the emerging quantum devices and modeling, simulation and design of cryogenic CMOS integrated ultra-scaled devices, circuits and systems for quantum computing.

4. Half Day: More Efforts to Developing High-Performance PLLs with Jitter Reduction Approaching Sub-10fs

Instructor(s):
- Yong CHEN, Nick (Associate Professor, University of Macau, Macau, China)

Abstract/Information:
This tutorial will present how to realize the simultaneous reduction of jitter and spur of the recent phase-locked loops (PLLs) being applied to ultra-high-speed communication systems, involving the past, present, and future of devising various circuit techniques. Next, the key limitations of jitter-spur performance for the classical PLLs will be studied and summarized, and how to break jitter-spur tradeoffs in different PLL variants exhibiting better figure-of-merit will be elaborated via several design examples fabricated in the CMOS process. Then, the potential paths to continuously pursue ultra-low jitter by fully leveraging the architectural advantages of every PLL will be summarized and discussed.

5. Half Day: Energy-Efficient AI-Native Wireless Communication Systems

Instructor(s):
- Rodney Martinez Alonso (Senior Researcher, KU Leuven and Ghent University (Belgium))
- Abdel Martinez Alonso (TechIdea Co., Ltd. (Japan))

Abstract/Information:
Artificial Intelligence is revolutionizing different areas of our lives. Indeed, Artificial Intelligence could be a major disruptive change in the way we design, standardize and exploit communications systems. A novel paradigm where the communication system is natively powered by Artificial Intelligence is presented in this tutorial. We also emphasize the challenges for AI-accelerators and ASIC design in terms of the computational performance and energy efficiency demanded by AI-native communications systems.

6. Half Day: Advanced Mixed Signal Concepts and Circuit Innovations Exploiting Active Bulk-Driven Techniques using 22nm FD-SOI CMOS Technology (22FDX)

Instructor(s):
- Marcel Runge (TU Berlin, Germany)
- Enne Wittenhagen (TU Berlin, Germany)
- Friedel Gerfers (TU Berlin, Germany)

Abstract/Information:
This tutorial starts with an in-depth introduction to the fully-depleted silicon-on-insulator technology (FD-SOI), normal techniques and flipped-well transistors and including all relevant technology parameters of the bulk node. Next an overview of the most recent design innovations in the field of analog and mixed-signal circuits and systems employing static or dynamic transistor-body biasing techniques are presented. Cutting edge circuit performance in terms of DC gain, bandwidth, linearity and power-efficiency is mathematically analyzed and verified by simulations and measurements when taking advantage of dynamic as well as static body-biasing architectures.

7. Half Day: Tensor Regression: Methods and Applications

Instructor(s):
- Yipeng Liu (Professor, University of Electronic Science and Technology of China (UESTC), Chengdu, China)
- Jiani Liu (Associate Professor, Xidian University, Xi'an, China)

Abstract/Information:
Regression analysis is a key area of interest in the field of data analysis and pattern recognition, which is devoted to exploring the dependencies between variables. For example, one can predict the future climate state from previous recordings or infer human age from their corresponding facial images. However, traditional modeling methods rely on representation and computation in the form of vectors and matrices, where the multidimensional signal needs to be unfolded for subsequent processing. The multilinear structure would be lost in such vectorization or matricization, which leads to suboptimal performance.

Tensors, as high-dimensional extensions of vectors, are considered natural representations of high-dimensional data. Driven by the recent advances in applied mathematics, it is natural for us to move from classical matrix-based methods to tensor-based methods for better performance and dimensionality reduction. In many fields, such as sociology, climatology, geography, economics, computer vision, chemometrics, and neuroscience, tensor regression has been widely employed and proven useful. This tutorial will provide you with a thorough overview of tensor-based regression methods and their applications. It is intended for researchers, developers, engineers, students, and people interested in gaining an overall understanding of tensor-based learning methods and their applications in data processing.

8. Half Day: Using Neural Networks to Optimize the Design of Analog and Mixed-Signal Circuits and Systems

Instructor(s):
- José M. de la Rosa (Professor, CSIC/University of Seville, Spain)

Abstract/Information:
This tutorial shows how to use Artificial Neural Networks (ANNs) for the optimization and automated design of analog and mixed-signal circuits. A survey of conventional and computational-intelligence design methods is given as a motivation towards using ANNs as optimization engines. A step-by-step procedure is described, explaining the key aspects to consider in our approach, such as dataset preparation, ANNs modeling, training, and optimization of network hyperparameters. As an application, two case studies at different hierarchy levels are presented. The first one is the system-level sizing of Sigma-Delta Modulators (ΣΔMs), where ANNs are combined with behavioural simulations to generate valid circuit-level design variables for a given set of specifications. The second example combines ANNs with electrical simulators to optimize the circuit-level design of operational transconductance amplifiers.

The presented methodology is described in a didactic way, and the contents are organized to learn the fundamentals and practical considerations behind the use of ANNs for automated design of analog circuits. No prerequisites are needed and the tutorial contents are organized and addressed for a general audience attending ISCAS.

9. Half Day: How to Model the Training and Inference of Analog-Based In-Memory Computing (AIMC) Systems

Instructor(s):
- Corey Lammie (IBM Research – Rüschlikon, Zürich, Switzerland)
- Manuel Le Gallo (IBM Research – Rüschlikon, Zürich, Switzerland)
- Malte Rasch (Sony AI Zurich, Switzerland)
- Kaoutar El Maghraoui (IBM Research – Rüschlikon, Zürich, Switzerland)

Abstract/Information:
AIMC is a promising approach to reduce the latency and energy consump6on of Deep Neural Network (DNN) inference and training. However, the noisy and non-linear device characteristics, and the non-ideal peripheral circuitry in AIMC chips, require adapting DNNs to be deployed on such hardware to achieve equivalent accuracy to digital computing. While traditional SPICE-based simulations can be used to model these systems, they require a significant number of resources, and are typically not feasible to run for large and complex DNNS, such as Large Language Models (LLMs) that currently dominate the Deep Learning (DL) landscape. Instead, customized simulation frameworks can be used to efficiently and accurately model key circuit and device behavior. The IBM recently released IBM Analog Hardware Acceleration Kit (AIHWKit), freely available at https://github.com/IBM/aihwkit, is one such framework capable of performing inference and training of DNNs using AIMC. In this tutorial, we provide a deep dive into how inference and training can be performed using the AIHWKit, and how users can expand and customize AIHWKit for their own needs.

Participants will be equipped with practical skills to model the training and inference of complex analog in-memory computing systems, using models developed from experimental data.

10. Half Day: Machine Learning for Automated Physical Design

Instructor(s):
- Ioannis Savidis (Associate Professor, Drexel University, Philadelphia, PA, USA)

- Pratik Shrestha (Associate Professor, Drexel University, Philadelphia, PA, USA)

Abstract/Information:
Electronic design automation (EDA) is a crucial process in the development of electronic systems, but it can be time-consuming and labor-intensive. Machine learning, particularly deep learning, has the potential to significantly improve the accuracy, speed, efficiency, and reliability of EDA tasks such as circuit simulation, layout design, and optimization. In this tutorial, we will provide a structured overview of current research on the application of machine learning in EDA, including key concepts, use cases, design phases, representation structures, and problem formulations. We will also discuss the formats and organizational structures for circuit data that are commonly used in this field. By the end of the tutorial, attendees will have a better understanding of the state of the art in machine learning for EDA and will be equipped with the knowledge and tools to pursue their research in this area.

11. Half Day: New Era of Artificial Intelligence: Unleashing the Power of Large Models in Visual Applications

Instructor(s):
- Jiaying Liu (Associate Professor, Peking University)
- Wen-Huang Cheng (Professor, National Taiwan University)
- Shuai Yang (Research Assistant Professor, Nanyang Technological University)

Abstract/Information:
In today's rapidly advancing technological landscape, the significance of large-scale vision generative and foundation models has never been more pronounced. These models represent a pivotal leap forward in our ability to understand and manipulate visual information. With applications spanning from creative fields like art and entertainment to critical domains like medical imaging and autonomous systems, these models have the potential to revolutionize how we interact with and interpret visual data.

However, the transition from theoretical excellence to practical implementation in the real world is fraught with intricacies. Closing the gap between their inherent potential and tangible applications remains a significant challenge. This raises the pivotal question: how can we systematically construct and effectively employ these large models, and can they, in turn, serve as a wellspring of inspiration and support for other tasks, such as image processing and multi-model applications? This tutorial is designed to offer a clear roadmap, illuminating both the promise and potential challenges associated with leveraging large-scale models to address diverse challenges across various domains.

12. Half Day: Hardware Security for Biomedical Circuits and Systems

Instructor(s):
- Ibrahim (Abe) M. Elfadel (Professor, Khalifa University, Abu Dhabi, UAE)

Abstract/Information:
The objective of this tutorial is to give the ISCAS audience an up-to-date overview of hardware security challenges in biomedical circuits and systems. The targeted audience is the ISCAS community of professionals and graduate students who are interested in the cybersecurity of biomedical circuits and systems, including implantable medical devices, wearable drug delivery systems, and neurostimulators. More specifically, the tutorial will focus on the hardware security

challenges of such devices and the ways to achieve a hardware root of trust for their long-term operation, especially in the case of implantable devices. Topics of particular interest include protection of biomedical integrated circuits through logic locking, resiliency against hardware trojans, and countermeasures against side channel attacks. Emerging embedded system design frameworks that are secure by construction, e.g., zero-trust methodologies, will be highlighted in terms of their relevance to securing the embedded systems of biomedical devices. The tutorial will include hands-on experiments on the Chipwhisperer hardware hacking platform, and attendees will get the opportunity to implement power side channel attacks to reveal authentication and access crypto keys on microcontrollers that are commonly used in embedded biomedical devices.

13. Half Day: Towards Battery-free and Low-cost Distributed Sensor Node: from Novel IC Approaches to System-level Industrial Design

Instructor(s):

- Orazio Aiello (Assistant Professor, the University of Genova)
- Roberto La Rosa (Research Senior Staff Member, STMicroelectronics, Catania)

Abstract/Information:

The vision of a world where pervasive integrated electronic systems are fully interconnected to collect, process, and exchange information leads to a significant growth trend in the global smart sensor market. However, powering Internet of Things (IoT) infrastructures of one trillion nodes with batteries poses considerable maintenance and management costs. In the framework of this increasing trend, this tutorial will highlight innovative circuital and systems-level strategies and techniques to drastically reduce power consumption and build battery-less and energy-autonomous electronic devices.

The first part of the tutorial focuses on the low-cost and low-power consumption requirements for energy-efficient IC design. These demand a small area, low design effort, digital-like shrinkage across CMOS generations, and design/technology portability. Moreover, the possibility to exploit the digital (automated) design flow even for analog building blocks can dramatically reduce the design effort of any system-on-chip enabling aggressively supply-voltage scaled and/or regulator-less building blocks that can be powered directly from energy harvesters. The second part of the tutorial will show a system-level industrial overview. In particular, it explores the research progress in sustainable wireless sensor nodes that require minimal or no maintenance. Additionally, how RF power transfer (WPT) can be a convenient way to remotely power wireless nodes, especially if installed in hard-to-reach places, will be shown.

WiCAS-YPCAS Event

WiCAS co-chairs of ISCAS 2024:
Yoko Uwate, Tokushima University
Maria Trocan, ISEP
Wang Bo, Singapore University of Technology and Design (SUTD), Singapore

YPCAS chair of ISCAS 2024:
Fidel Makatia, Autodesk, Kenya

Join us for an insightful panel discussion featuring from industrial to academic to apply agile leadership to navigate the challenging situations in the dynamic world. The invited panelist will share their personal journeys, strategies, and practical tips on how they've embraced agility to break barriers, overcome challenges, lessons learnt and successful stories.

Agile-Leadership
18:30 - 18:35 Opening
18:35 - 18:50 Ice break gaming
18:50 - 19:20 Panel discussion
19:20 - 19:25 Feedback
19:25 - 19:30 Closing
19:30 - 21:00 Cocktail networking discussion

Panellists:

Dr. Zhu Yao
Head of Department in Institute of Microelectronics, Singapore

Marcus Janke
Infineon Technologies AG Munich, Germany

Dr. Chi-Seng Lam
YPCAS chair,
DEI committee CAS,
University of Macau

Dr. Yi (Estelle) Wang
Continental Automotive

Moderator:

Eugene Seah
Abundance Life Coach

Zhu Yao is the Head of MEMS department in Institute of Microelectronics (IME), A*STAR Singapore. Her current research interests include MEMS devices for sensing, actuating and wireless communication applications. Zhu Yao received her Ph.D. degree from Nanyang Technological University in 2015. She is actively involved in IEEE societies such as associate editor for IEEE MEMS Journal, committee member of IEEE Solid State Circuit Society Singapore Chapter & IEEE Nanotechnology Technical Council, technical sub-committee member of IEEE IEDM 2023 and IEEE MEMS 2023. She is the recipient of SEMI MEMS & Sensors Industry Group Emerging Leaders Awards 2022.

Marcus Janke
Since 1989: Analyses smart cards with the focus on security and privacy topics
Since 1991: Conceptions, development and realizations of smart card systems
Since 1992: Author and consultant with numerous related publications and lectures on international conferences in the area of security
1997: Diploma-Degree in Electronics (Dipl-Ing)
1997-1999: Newtec Hamburg for OMRON
1999-today: Infineon Technologies AG Munich

Current Position
* Fellow Security at Infineon, responsible for consideration of attacks on security ICs and automotive ICs
* Advisory in several international working groups like JHAS of Common Criteria, V2X of automotive section and FIDO of identification systems,
* Trainer for Automotive Cyber Security (ACS) at German Association of the Automotive Industry (VDA)

Chi-Seng LAM received the Ph.D. degree in electrical and electronics engineering from the University of Macau (UM), Macau, China, in 2012. He completed the Clare Hall Study Programme at the University of Cambridge, Cambridge, U.K., in 2019. In 2013, he was a Postdoctoral Fellow with The Hong Kong Polytechnic University, Hong Kong, China. He is currently an Associate Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI, Institute of Microelectronics, and Department of Electrical and Computer Engineering in Faculty of Science and Technology, UM. He has coauthored or co-edited four books and more than 180 technical journals and conference papers. He holds six U.S. and five Chinese patents. His research interests include power converters, power quality compensators, photovoltaic energy generation system, power management integrated circuits, and wireless power transfer.

Dr. LAM was a recipient or co-recipient of the IEEE PES Chapter Outstanding Engineer Award in 2016, the Macao Science and Technology Invention Award (Third Class and Second Class) in 2014 and 2018, respectively, and the Gold Medal of 48th International Exhibition of Inventions of Geneva in 2023. He is currently the Chair of the Young Professionals in Circuits and Systems (YPCAS) of IEEE CASS, Chair of the IEEE Macau IES Chapter and the Secretary of the IEEE IES Technical Committee on Power Electronics. He currently serves as an Associate Editor for the IEEE Transactions on Industrial Electronics, the IEEE Open Journal of the Industrial Electronics Society, and the IEEE Access. He was awarded 2021 IEEE Access Outstanding Associate Editor and the 2022 IEEE Transactions on Industrial Electronics Distinguished Reviewer. He was also recognized as the world's top 2% scientist for 3 consecutive years (2020, 2021, 2022) by Stanford University and Elsevier.

Dr. Yi (Estelle) Wang has been working as Head of Product Cybersecurity & Privacy Office (PCSO) Singapore at Continental Automotive since July 2016 (with a 2008 Ph.D. degree from Nanyang Technological University, Singapore). Dr. Wang is leading three teams: the automotive advanced

research and governance team, consulting and engineering team, and the security operations team. In addition, she is with deep knowledge of ISO/SAE 21434 and UNECE R155/R156 based on physically participating in working group meetings. She is an expert with cybersecurity industrial standards, e.g., ISO 2700x and ISO 26262. She is familiar with data protection and privacy regulations: GDPR and Asia regional regulations (Singapore PDPA and Chinese PIPL). Advanced leading research topics are including but not limited to applied post quantum cryptography, applied lightweight cryptography, cybersecurity for artificial intelligence (adversarial model), embedded security for IoTs, data anonymization for personal privacy.

Dr. Wang is honored with “Top Women in Security ASEAN 2021” 2021 and 2022 (Singapore, Phillips, Indonesia, Malaysia, Cambodia, and Thailand), “Top Women in Security – Singapore Country Award” and “Top 20 Women in Cybersecurity Singapore 2020” by Public Security Society. She brought the know-how to the Singapore Cybersecurity ecosystem through guest lectures with the Singapore Institute of Technology in 2019. She is motivated to be valuable in various domains, actively contributing to her company, the IEEE non-profit community, and the Singapore eco-system. She firmly believes that investing effort in mentoring and coaching young talents will contribute to creating a better future.

With more than 20 years of experience in various embedded security topics, she is active in academic activities, has published more than 53 international top journal/conference papers, and holds 13 industrial patents. She was Chair of the IEEE Circuit and System Society (CASS) chapter Singapore 2022-2023, Associate Editor of IEEE Transactions on Circuit and System II 2020-2022, and Chair for IEEE Standard of Hardware Security under IEEE Circuits and Systems Society Standards Activities Subdivision.

Eugene Seah calls himself a reformed corporate zombie, who found his life purpose in 2014 when he lost his job.Since discovering his life purpose, he has been invited round the world to share his story (including Moscow, Dubai, Shanghai, Florida, and even Pyongyang!), and also appeared multiple times on radio, TV and the newspapers.

In his keynotes and coaching programs, he combines his unique experience of regional corporate leadership with NLP (neurolinguistic programming) psychological principles, as well as practical and timely business case studies.

He graduated from NTU specialising in effective communications, and won a scholarship from SGX (Singapore Exchange) and a Gold award from The Business Times Singapore for his contribution to the investor relations industry.

For the last 10 years he has gained a reputation as a highly engaging, humorous and mind-opening speaker and coach, whose mission is to help the world achieve a life of abundance, overflowing with joy and fulfilment.

Embedded Workshops

Embedded Workshops Chair of ISCAS 2024:
Fakhrul Zaman Rokhani, Universiti Putra Malaysia, Malaysia

Four embedded workshops at ISCAS 2024, coinciding with the celebration of the CAS Society 75th anniversary, are organised to showcase the excellence of CASS members' work on frontier topics - (i) Climate change, (ii) Technology for the elderly, and (iii) Information security, and (iv) Autonomous Mobility CAS. These topics are of increasing relevance in today's world.

Firstly, the realities of climate change are undeniable, and many communities are facing the consequences of unpredictable events that are extreme (such as floods) or slow-onset (such as the accelerated temperature increase that upsets ecosystems). In this context, it is imperative for all sectors, including the electronics industry, to help adapt to climate change and to mitigate their contributions to increasing temperatures. Secondly, the rapidly aging populations are no longer limited to post-industrialized nations but are also seen in many populous countries such as India and China - in this context, it becomes important to develop solutions to assist the lives of these demographics. Thirdly, the ubiquity of information and communications technologies, from social media to sensor networks, throws open the huge challenge of data security, privacy, and integrity. There is a need to strengthen these regulatory frameworks while also developing appropriate technological solutions. Finally, the progressive evolution of electronic systems-based autonomous vehicles are going beyond merely controlling engines, into the safety, driving assistance, and communications domains. Ensuring the seamless operation of autonomous vehicles mandates highly dependable circuits and systems encompassing areas like artificial intelligence (AI), sensing, signal processing, and V2X communications.

These workshops are organized by researchers and prominent speakers with solid experience adapting their work to these topics. Further details of each topics are discussed below.

1. EW1: Climate Change

Chair: Dr Balwant Godara (Political advisor at SWA, the UN-hosted partnership on water USA/Switzerland)

Abstract/Information:
The overall aim of the Embedded Workshop on Climate Change is to advance the ICT community's understanding of the role of circuits and systems in climate – both as part of the solutions to adapt to the new reality of climate change and as contributors to aggravations in climate change. Thereafter, participants will consider how to better integrate climate action into their work on circuits and systems.

The workshop is timely, since the need has never been greater to design, implement and scale up high-impact actions to address climate change. It will make use of the high scientific credibility, quality and visibility of ISCAS to push the climate agenda higher in the community working on information and communications technologies, including circuits and systems. The workshop builds on two successful editions of the EmC^2 workshop organised by the IEEE Circuits and Systems Society – in 2022 and 2023.

The workshop aims to give the following outcomes:

- A deeper understanding of how solutions based on circuits and systems can help adapt to climate change and mitigate their own harmful contributions to climate change.
- Specific illustrations of the above, using case studies and examples that show that the climate future could also be the digital future, in the best possible way.

- Exploration of how participants can integrate climate change into their own research efforts.

All these will be documented in the form of a white paper, carrying on the trend established via the two EmC^2 workshops. This paper will be widely disseminated within CASS and IEEE, to inform and inspire other researchers.

2. EW2: Technology for the Elderly

Chair: Mohd Nazim Mohtar (Universiti Putra Malaysia, Malaysia)

Abstract/Information:
The Embedded Workshop on technology for the elderly, GeronCAS, at ISCAS 2024 has the overarching goal of sustaining and fostering interest in the continuous development of technology designed to empower systems for managing the care of the elderly. Through this workshop, we aim to cultivate a heightened focus on technology development specifically tailored to address the needs of seniors within the Circuits and Systems (CAS) society. GeronCAS aspires to position itself as the premier reference gathering for scientists and industry stakeholders actively involved in the creation of cutting-edge technologies and solutions dedicated to enhancing the well-being of seniors and the elderly. By providing a dedicated space for collaboration, knowledge exchange, and innovation, GeronCAS aims to play a pivotal role in advancing the field of gerontechnology within the CAS community.

3. EW3: Information Security

Chair: Shivam Bhasin (Nanyang Technological University, Singapore)

Abstract/Information:
The Embedded Workshop on information security at ISCAS 2024 aims to advance understanding of circuits and systems' role in supporting security for emerging technologies like Quantum Computing, AI, Smart End Devices, and Cloud Computing. Each technology faces unique security challenges, requiring tailored solutions. The workshop will discuss these challenges and highlight how circuit and system innovations contribute to their growth, while also identifying common security concerns across these technologies to encourage the development of optimized and innovative solutions applicable to a spectrum of emerging technologies. Outcomes include providing an overview of security challenges, existing circuit-level solutions, identifying coherence in security issues, and ultimately informing and inspiring researchers through a white paper.

4. EW4: Autonomous Mobility CAS

Chair(s): Kyung Ki Kim (Daegu University, Korea) & Preet Yadav (NXP Semiconductors, India)

Abstract/Information:
This year's AutoCAS Workshop continues to see growing interest in Autonomous Mobility Circuits and Systems (AutoCAS) as the technological front advances rapidly and the evolution of autonomous vehicles based on electronic systems continues. Beyond engine control, they play an essential role in safety, driver assistance, and communications. Highly reliable circuits and systems covering areas such as artificial intelligence (AI), sensing, signal processing, and V2X communications are essential to ensure smooth operation of autonomous vehicles.

In this changing environment, new electronic systems aim to configure the vehicle's behavior through software in a more intuitive way. The field of circuit and system design tailored for autonomous mobility represents an important investment focus for semiconductor companies and is forecast to have significant revenue and growth trajectories. Our CAS community needs expanded

opportunities for interaction and collaboration with experts exploring new trends in autonomous mobility CAS. This is essential to foster technological progress and dominance.

Accordingly, AutoCAS 2024 is ready to showcase pioneering contributions that address CAS-centric challenges arising from autonomous mobility components such as memory, sensors, ECUs, and deep neural network (DNN) processors. This workshop is intended to be a connecting point for researchers to gain insight into cutting-edge methodologies and determine their pros and cons. This valuable exposure prepares them to innovate and refine circuits and systems while imagining the needs of complex vehicles. The structure of the workshop will include a single plenary track featuring insights from six leading figures from industry and academia.

Building on this content, this year's AutoCAS Abstract has been updated to reflect last year's achievements and this year's technical challenges and expectations. As technology continues to advance, we expect the AutoCAS community to be at the forefront of innovation and drive the advancement of circuits and systems for a new era of automobiles.

Cross-Society Special Session

Cross Society Special Session:
Flexible Circuits & Systems for the Era of Everything Intelligence

The IEEE International Symposium on Circuits and Systems (ISCAS) 2024, set to take place in Singapore from May 19 to 22, focuses on "Circuits and Systems for Sustainable Development". A notable highlight is the Cross Society Special Session dedicated to Flexible Circuits & Systems, pivotal for the Era of Everything Intelligence, in collaboration with the IEEE Electron Devices Society (EDS)This session underscores the significance of adaptable and versatile platforms, termed Smart Interfaces, that enable intelligent interplay among humans, machines, and the environment, reflecting the rapid technological advancements of our time. The mirror session will be held at the IEEE International Flexible Technology Conference (IFETC) 2024 from September 15 to 18 in Italy.

The discussion will span across several key topics, including wearable and implantable devices, sensor integration, energy harvesting, bioelectronics, human-machine interfaces, IoT-compatible electronics, printed electronics, machine learning applications, novel materials, and security concerns in smart interfaces. Such diversity underscores the session's comprehensive approach to exploring flexible systems' potential to revolutionize various life aspects.

The following papers has been accepted by this session:

1. 1024-Channel Neurostimulation System Enabled by Photolithographic Organic Thin-Film Transistors with High Uniformity by Bowen Liu, Yangkun Hou, Yueshan Qin, Jiwei Zou, Hanbin Ma, Yongpan Liu, Huazhong Yang, Xueqing Li, Chen Jiang
2. Squeeze-Excite Fusion Based Multimodal Neural Network for Sleep Stage Classification with Flexible EEG/ECG Signal Acquisition Circuit by Shuailin Tao, Jinhai Hu, Wang Ling Goh, Yuan Gao
3. A Large-Area LTPS-TFT-Based Bi-Directional Biomedical Interface with Process-Invariant In-Pixel Biopotential-to-Digital Converters by Hanbo Zhang, Yuqing Lou, Zhihang Zhang, Yongfu Li, Fakhrul Zaman Rokhani, Guoxing Wang, Jian Zhao
4. An Ultra-Low Power Wearable Sensing System with a Highly Sensitive Three-Dimensional LIG Sensor and Energy-Efficient Time Domain Readout by Siyuan Xu, Huiru Yang, Longhuang Li, Yiyang Du, Huaiyu Ye, Huan Hu
5. A 2.5 kHz 50.57 dB Linearized VCO ADC Using 6 µm LTPS TFTs by Wangzilu Lu, Jiajie Huang, Chao Wang, Ting Zhou, Yang Zhao, Jian Zhao, Yongfu Li

This session not only showcases the latest innovations but also sets the stage for future research directions. It emphasizes the importance of interdisciplinary collaboration in advancing flexible circuit and system technologies, crucial for realizing the vision of a seamlessly interconnected and intelligent world. These papers will be invited for possible publication in the IEEE Journal on Flexible Electronics (J-FLEX), indicating their significant contribution to the field.

The paper submission deadline to the mirror session in IFETC 2024 will be April 30th, 2024. This further extends this collaborative effort, inviting more contributions to this dynamic field.

Organizers:

Jian Zhao, Shanghai Jiao Tong University
Leilai Shao, Shanghai Jiao Tong University
Yongfu Li, Shanghai Jiao Tong University
Yuhang Zhang, Shanghai Jiao Tong University
Feng Zhang, IME of the CAS, China
Chen Jiang, Tsinghua University
Xinmiao Zhang, Ohio State University

CASS Standards Association Workshop

CASS Standards Association Workshop Chair of ISCAS 2024:
General Chiar(s):
Yong Lian (York University, Canada) & Liebin Zhao (Xinhua Hospital Affiliated to SJTU, China)
TPC Chair(s):
Yongfu Li (Shanghai Jiao Tong University, China), Boon Chong Ang (Intel, Malaysia), Yang Zhao (Shanghai Jiao Tong University, China), Yong Yin (Shanghai Children's Medical Center, China)

The First IEEE CAS Standards Workshop, in collaboration with the IEEE International Symposium on Circuits and Systems (ISCAS2024), is a premier event where participants will be immersed in the development of international technology standards. By participating, you will delve into the IEEE SA Standards Development Process, explore the path to becoming an IEEE Fellow through standardization activities, and discover the capabilities of IEEE Dataport for data sharing and competitions. Our distinguished panel of IEEE members, medical experts, AI researchers, and standardization specialists are eager to guide you through the intricate landscape within IEEE CASS. Engage in captivating sessions, interactive discussions, and practical case studies to gain valuable insights into how international standards empower new technologies such as chiplet, data privacy, interoperability, and healthcare. Join industry leaders and experts who are shaping the standards that drive technological innovation and ethical AI implementation in healthcare and beyond.

Morning Program (Perspectives from IEEE Distinguished Guests)

Speaker	Affiliation	Topic
Tom Thompson	IEEE SA Program Manager	IEEE SA Standards Development Process
Qinfen Hao	IEEE P3468 Working Group Chair	Introduction to P3468 – Chiplet Interface Circuit Working Group
Don Tan	IEEE Fellow Committee Past Chair	IEEE Fellowship through IEEE Standards Activities
Rakesh Kumar	IEEE Dataport Steering Committee Chair	IEEE Dataport
Plenary Discussions: Tom Thompson, Rakesh Kumar, Qinfen Hao, Moderator: Boon Chong Ang		

Afternoon Program (Perspectives from Medial Doctors)

Speaker	Topic
Liebin Zhao	Digital dividend or Digital Divide: Reflection on User Perspectives in the Development and Standardization of Digital Health Technologies
Yin Yong	The Origin and Breakthrough of the Intelligent Respiratory Sounds
Xiang Long	Standardization of medical artificial intelligence technology from the perspective of critical intensivists
Xiaoli Tang	Design of a standardized innovative device for multimodal sensory stimulation bundles for preterm infants
Plenary Discussions: Jiajun Yuan, Wenyi Luo, Lanping Wu, Kefei Wu, Jinqing Zeng, Moderator: Yong Lian	

3D Integration & Advanced Packaging Workshop

Workshop Chair of ISCAS 2024:

Xuanyao Fong, National University of Singapore, Singapore
Anh Tuan Do, IME, A*STAR, Singapore

As CMOS process advancements slow down, the chiplet design approach and its associated technologies have garnered significant attention due to their potential for improving manufacturing yield, reducing costs and offering extensible SOC architecture. This however will require radical shifts in chip design methodologies. This session will examine the latest developments in chiplet technology, encompassing SOC architectures built upon chiplet frameworks, chiplet interface circuits (such as D2D interconnect technology), chiplet EDA tools, and cutting-edge packaging techniques tailored for chiplet integration. We will also discuss the challenges impacting chiplet technology, including varying standards, complexities in designing, testing and thermal management of chiplet-based implementation.

	Title	Speaker	Time
1	Embracing a New Chapter for 3D IC Design with Generative AI: Optimize from Architecture Conceptual Level to Signoff	**Erick Chao,** Senior Software Architect, Cadence Design Systems, Inc	9.00-9.22
2	Chiplet Interface Circuit Design Challenge and Standards Development	**Qinfen Hao**, President, Wuxi Institute of Interconnect Technology, Co. Ltd., China.	9,22-9.45
3	Opportunities and Challenges in general purpose CPU design based on chiplet architecture	**William Fan,** CEO, M2 Semiconductor Ltd., China.	9.45-10.07
4	Heterogeneous Chiplet Integration Technologies for AI Driven Accelerated Computing	**Surya Bhattacharya,** SiP Director, Institute of Microelectronics, A*STAR, Singapore	10.07-10.30
Tea break			10.30-11.00
5	Computing: The Power of Die-to-Die Interfaces and Chiplet Architecture	**Yu WANG** , Sr. Analog Design Manager, Kiwimoore, Semiconductor Co. Ltd, Shanghai, China.	11.00-11.22
6	Signal/Power Integrity and Multiphysics Analysis for Interconnects of Chiplet	**Bo Pu,** Vice President, Ningbo DeTooLIC Technology Co., Ltd, Ningbo, Zhejiang, China	11.22-11.45
7	Opportunities and challenges faced by advanced chiplet interconnection technology	**Shujuan Liu**, Engineer, Hubei Yangtze Laboratories, China.	11.45-12.07
8	Radiative cooling via the integration of heat spreader and radiator in electronic device	**Siah Chun Fei,** Research Fellow, National University of Singapore, Singapore.	12.07-12.30
Lunch			12.30-13.30

IEEE ISCAS PhD Forum

The IEEE ISCAS Ph.D. Forum, a new initiative by the IEEE Circuits and Systems (CAS) Society, symbolizes a significant leap forward in supporting and recognizing the academic endeavors of Ph.D. students within the circuits and systems community. This forum is not merely an event; it is a testament to the IEEE CAS Society's commitment to nurturing the intellectual growth and professional development of the next generation of pioneers in the field. With the extension of the IEEE CAS Society Pre-doctoral Grant to the IEEE ISCAS Pre-doctoral Grant, our society recognizes the exemplary academic achievements and contributions of young members, fostering an environment of innovation and leadership.

Held in conjunction with IEEE ISCAS, the global flagship conference within the IEEE CAS Society, the Ph.D. Forum provides a unique stage for Ph.D. students to present their research through engaging oral and poster sessions. This hybrid event is crafted to facilitate a dynamic interchange of ideas among a diverse array of participants, including peers, mentors, and industry stalwarts. The forum aims to be a crucible where doctoral research receives critical evaluation, fostering academic excellence and facilitating the transition of cutting-edge research from academia to industry.

The first IEEE ISCAS forum has received participation from 32 different universities, and 40 Ph.D. students being accepted, highlighting its global reach and diversity. Notably, 23 Ph.D. students have publications in ISCAS 2024, and 33 Ph.D. students have past publications in IEEE CAS journals and conferences, highlighting the sustained commitment within the community. The inclusion of 7 newcomers showcases the forum's inclusivity and appeal to budding researchers.

Recognizing the financial challenges faced by students, the IEEE CAS Society demonstrates commendable support through travel grants, ensuring that financial constraints do not hinder participation in this premier event. This initiative is part of a broader strategy to make the forum accessible to all deserving candidates, promoting equity and inclusivity. The strategic decision to co-locate the forum with IEEE ISCAS not only amplifies its reach within the CAS Society community but also eliminates the need for additional registration, making it more accessible. The forum's alignment with IEEE ISCAS enhances its visibility and offers unparalleled networking opportunities, bridging the gap between academia and industry.

The forum also celebrates academic excellence through the IEEE ISCAS Pre-doctoral Grants, further motivating participants to strive for excellence. Plans to extend this successful format to other flagship CAS Society’s conferences signify a promising future for this initiative.

In conclusion, the IEEE ISCAS Ph.D. Forum embodies a confluence of academic rigor, innovation, and collaboration. It stands as a beacon of opportunity for doctoral students, offering a platform to showcase their work, receive valuable feedback, and contribute to the shaping of the future of circuits and systems. With its inclusive approach and commitment to fostering a vibrant academic community, the forum invites all eligible Young CAS Society’s members to participate in this enriching experience, paving the way for a future replete with discovery and technological advancement.

Organizing Committee

Yongfu Li, Shanghai Jiao Tong University, China
Yuhang Zhang, Shanghai Jiao Tong University, China
Yanan Sun, Shanghai Jiao Tong University, China
Yu Wu, University College London, UK
Bo Li, Xidian University, Chin

Student Design Competition

Student Design Competition Chair of ISCAS 2024:
Kea-Tiong (Samuel) Tang

The IEEE Circuits and Systems Society (CASS) is pleased to hold the 8th CASS Student Design Competition. The CASS Student Design Competition is a worldwide competition where undergraduate students will suggest and execute projects on electrical engineering and related areas. The focus is on finding a solution to a real-life problem based on circuits and systems. The competition takes place in three phases, the first at the chapter level, the second at the regional level, and the final at the world level. The final this year takes place during the 2024 IEEE International Symposium on Circuits and Systems (ISCAS 2024) in Singapore. Four finalists, one for each region – Region 1-7 (USA and Canada), Region 8 (Europe, Middle East, Africa), R9 (Latin America), and Region 10 (Asia, Australia, Pacific) will compete on the final stage!

The four finalists are:

Region 1-7 (USA and Canada)
Ghost in the Machine: High-Performance FPGA Implementation for Deep Learning Acceleration
Houston Chapter

Region 8 (Europe, Middle East, Africa)
FeatherTech
Kenya Chapter

R9 (Latin America)
Low Cost Interactive Embedded Device for Attention Training in Children with ADHD
Ecuador Chapter

Region 10 (Asia, Australia, Pacific)
A Wearable Cardiopulmonary Healthcare System For Real-Time Monitoring Of Multi-Modal Physiological Signals
Shanghai chapter

12th International Workshop on Computational Intelligence for Multimedia Understanding

Chair:
Maria Trocan, ISEP, France
Davide Moroni, Institute of Information Science and Technologies, National Research Council of Italy (CNR), Pisa, Italy
Behçet Uğur Töreyin, Informatics Institute, Istanbul Technical University (ITU), Istanbul, Turkey

The International Workshop on Computational Intelligence for Multimedia Understanding (IWCIM) is the annual workshop organized by the working group Multimedia Understanding through Semantics, Computation and Learning (MUSCLE) of the European Research Consortium for Informatics and Mathematics (ERCIM). This year, IWCIM takes place as a satellite workshop to IEEE ISCAS 2024, to be held in Singapore on May 19 - 22, 2024.

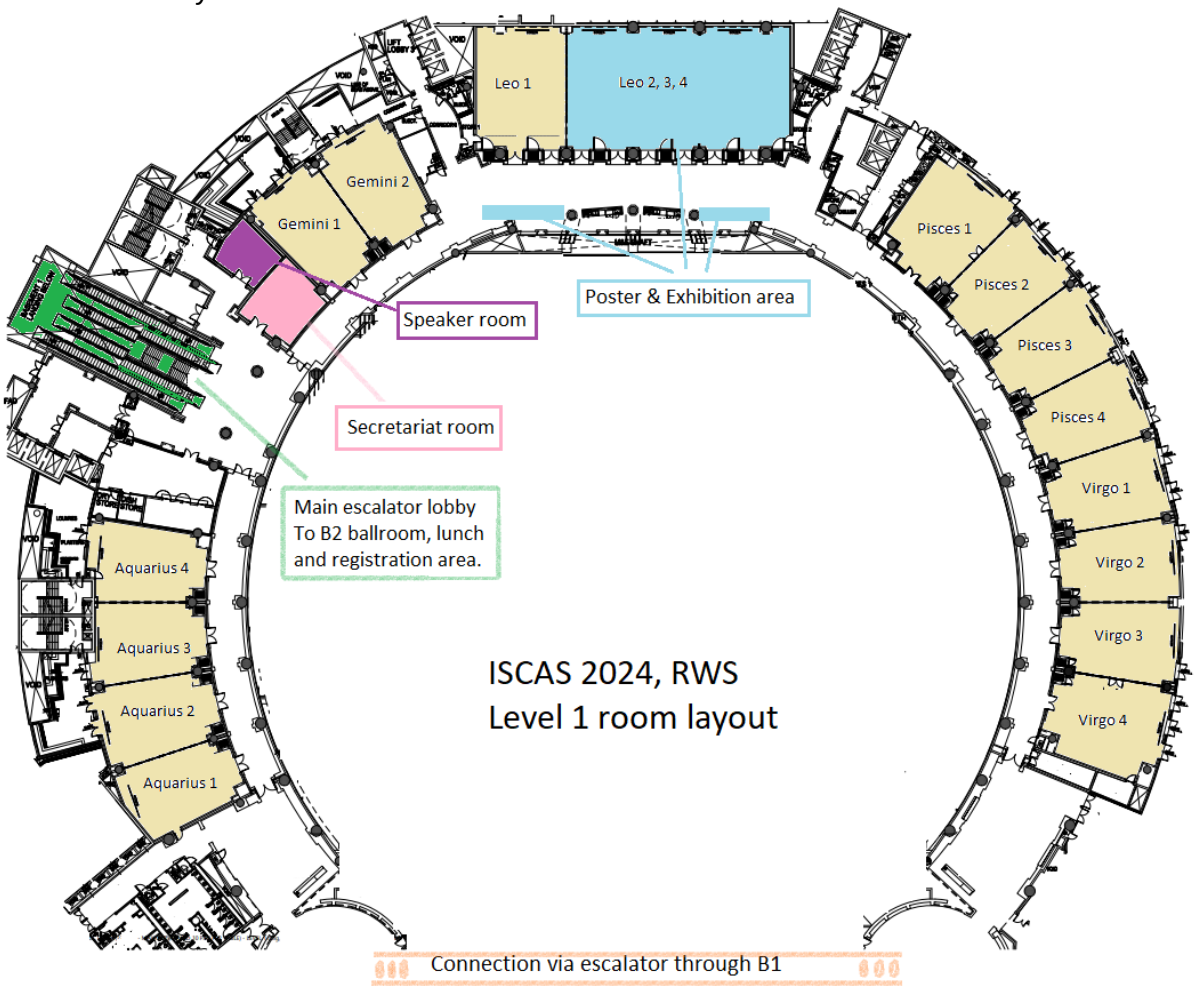
Multimedia understanding is an essential part of many intelligent applications in our social life, be it in our households, or in commercial, industrial, service, and scientific environments. Analysing raw data to provide them with semantics is essential to exploit their full potential and help us manage our everyday tasks. Nowadays, raw data usually come from a host of different sensors and other sources, and are different in nature, format, reliability and information content. Multimodal and cross-modal analysis are the only ways to use them at their best. Besides data analysis, this problem is also relevant to data description intended to help storage and mining. Interoperability and exchangeability of heterogeneous and distributed data is a need for any practical application. Semantics is information at the highest level, and inferring it from raw data (that is, from information at the lowest level) entails exploiting both data and prior information to extract structure and meaning. Computation, machine learning, statistical and Bayesian methods are tools to achieve this goal at various levels.

IWCIM 2024 includes the following topics:

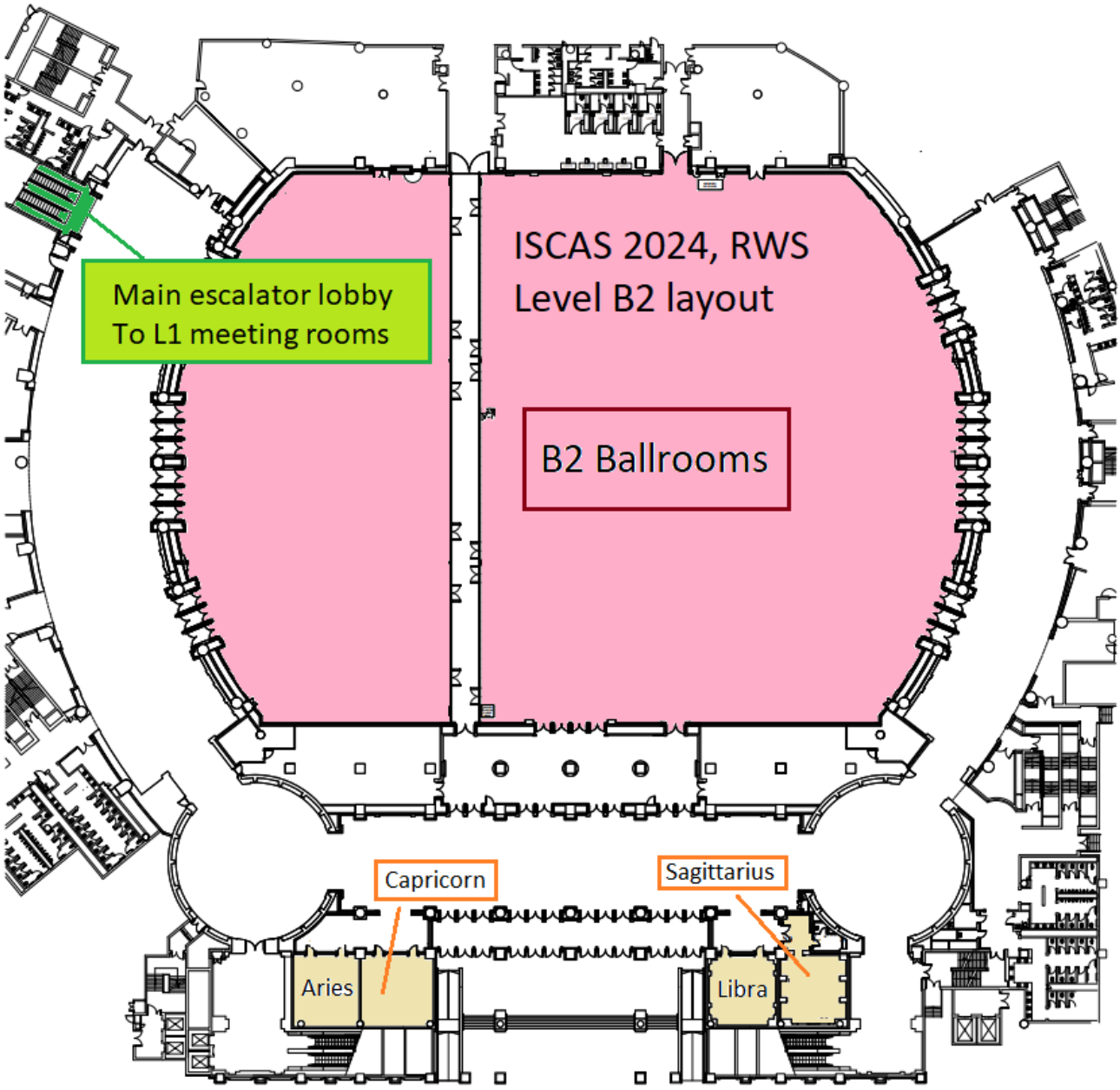
- Multisensory systems
- Multimodal analysis
- Cross modal data analysis and clustering
- Activity and object detection and recognition
- Text and speech recognition
- Multimedia labelling, semantic annotation and metadata
- Multimodal indexing and searching in very large data-bases
- Machine learning in multimedia understanding
- Attention based approaches for multimedia understanding
- Diffusion models for multi-modal data analysis
- Multi-modal data analysis in compressed domain and for remote sensing applications
- Multimedia and multi-structured data

Venue Map

Level 1: Room Layout



Level B2: B2 Ballroom



Program at a Glance

Time: UTC+8	Sunday, May 19		
07:45-08:30	**Registration** [Foyer of Taurus Room (Secretariat Room)]		
08:30-10:00	**Full-Day Tutorial** #1,# 2, #3 1. Mixed-Signal RF Transmitters (Instructor(s): David J. Allstot, Vanessa Chen, and Jeffrey S. Walling) [Room: Pisces 2]	**Half-Day Tutorial (Morning)** #1 1. More Efforts to Developing High-Performance PLLs with Jitter Reduction Approaching Sub-10fs (Instructor(s): Yong Chen (Nick)) [Room: Aquarius 1] 2. Tensor Regression: Methods and Applications (Instructor(s): Yipeng Liu, Jiani Liu) [Room: Aquarius 2] 3. Energy-Efficient AI-Native Wireless Communication Systems (Instructor(s): Martinez Alonso, Rodney, Martinez Alonso, Abdel) [Room: Aquarius 3] 4. Advanced Mixed Signal Concepts and Circuit Innovations Exploiting Active Bulk-Driven Techniques using 22nm FD-SOI CMOS Technology (22FDX) (Instructor(s): Marcel Runge, Enne Wittenhagen, Friedel Gerfers) [Room: Aquarius 4] 5. Using Neural Networks to Optimize the Design of Analog and Mixed-Signal Circuits and Systems (Instructor(s): José M. de la Rosa) [Room: Gemini 1]	N/A
10:00-10:30 10:30-12:30	2. Advanced Biomedical Imaging Technologies: Circuit Design and Techniques (Instructor(s): Yuanjin Zheng, Yongfu Li, Jian Zhao, Ka-Meng Lei) [Room: Pisces 1]		
12:30-13:30		**Lunch** [Venue: West Lobby, Foyer beside Aquarius 1]	
13:30-15:00	3. Integrated Devices, Circuits and Systems for Quantum Computing (Instructor(s): Andreas Fuhrer Janett, Christian Enz, Andrei Vladimirescu, Fabio Sebastiano, Edoardo Charbon, Joseph Bardin, Sorin Voinigescu, Domenico Zito) [Room: Leo 1]	**Half-Day Tutorial (Afternoon)** #3 1. How to Model the Training and Inference of Analog-Based In-Memory Computing (AIMC) Systems (Instructor(s): Corey Lammie, Manuel Le Gallo, Malte Rasch, Kaoutar El Maghraoui) [Room: Aquarius 2] 2. Machine Learning for Automated Physical Design (Instructor(s): Ioannis Savidis, Pratik Shrestha) [Room: Aquarius 3] 3. Towards Battery-free and Low-cost Distributed Sensor Node: from Novel IC Approaches to System-level Industrial Design (Instructor(s): Orazio Aiello, Roberto La Rosa) [Room: Aquarius 4] 4. Hardware Security for Biomedical Circuits and Systems (Instructor(s): Ibrahim (Abe) M. Elfadel) [Room: Gemini 1] 5. New Era of Artificial Intelligence: Unleashing the Power of Large Models in Visual Applications (Instructor(s): Jiaying Liu, Wen-Huang Cheng, Shuai Yang) [Room: Gemini 2]	N/A
15:00-15:30			CASS Blitz ISCAS2024 Edition [Room: Aquarius 1]
15:30-17:00			N/A
18:00-21:00	**Welcome Reception** [Venue*: Gardens By the Bay (Flower Field Hall and Water View Room)]		

#1 – Coffee break at 10:00-10:30; #2 – Lunch at 12:30-13:30; #3 – Coffee break at 15:00-15:30
* The venue is not located within the conference site. It takes about 20min for driving and 40min for public transportation from the conference site to there.

Time: UTC+8	Monday, May 20			
07:45-08:30	**Registration** [Foyer of Taurus Room (Secretariat Room)]			
08:30-09:00	**Opening Ceremony** [Venue: B2 Ballroom]			
09:00-10:00	**Keynote 1:** Aaron Thean, Deputy President (Academic Affairs) and Provost, National University of Singapore, Singapore [Venue: B2 Ballroom]			
10:00-11:00	**Keynote 2:** Gert Cauwenberghs, Professor, Co-Director of the Institute for Neural Computation, University of California San Diego, USA [Venue: B2 Ballroom]			
11:00-11:30	**Coffee Break**			**Poster/Demo** 1. Poster (11 Sessions) 2. Live Demo I [Room: Leo 2, 3, 4]
11:30-13:00	**Regular Sessions** 1. Amplifiers [Room: Aquarius 1] 2. Models & Methods for Non-Linear Circuits & Systems [Room: Aquarius 2] 3. Data Path & Arithmetic Circuits and Systems [Room: Aquarius 3] 4. Hardware Security for IoT, Circuits and Cyber-Physical Systems I [Room: Aquarius 4] 5. Wireline Communications [Room: Gemini 1] 6. Integrated Power Circuits & Charge Pumps [Room: Gemini 2] 7. Neural Interface Circuits & Systems I [Room: Pisces 1] 8. Neural Learning Systems: Optimizations & Applications I [Room: Pisces 2] 9. Learning-based Visual Signal Coding & Processing [Room: Pisces 3]	**Special Sessions** 1. Cross Society Special Session: Flexible Circuits & Systems for the Era of Everything Intelligence [Room: Pisces 4] 2. Inversion Coefficients & Ratio-based (gm/ID, gm/Cg, etc.) Design Methodologies [Room: Virgo 1] 3. Novel Hardware Implementation of Learning Algorithms in Deep & Spiking Neural Networks I [Room: Virgo 2] 4. RFIC & AI: Pioneering New Wireless Communications [Room: Virgo 3]	**Workshop/Other** 1. Student Design Competition [Room: Leo 1]	
13:00-14:00	**Lunch** [Venue: B2 Ballroom]			

Time: UTC+8	Monday, May 20 (Continue)			
14:00-15:00	**Keynote 3:** Sandro Carrara, Professor, Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland [Venue: B2 Ballroom]			
15:00-16:30	**Regular Sessions** 1. LDO Regulators [Room: Aquarius 1] 2. AI & ML Techniques for Non-Linear Circuits & Systems [Room: Aquarius 2] 3. Low Power Logic, Circuits & Architectures I [Room: Aquarius 3] 4. Digital Circuits, Systems & Architecture for Machine Learning I [Room: Aquarius 4] 5. Optical Communications [Room: Gemini 1] 6. Circuits & Systems for Energy Harvesting [Room: Gemini 2] 7. Neural Interface Circuits & Systems II [Room: Pisces 1] 8. Neural Learning Systems: Transformers & Applications I [Room: Pisces 2] 9. Image/Video Coding & Standardization [Room: Pisces 3]	**Special Sessions** 1. Optical & Wireless Communication & Sensing Technologies in Terrestrial & Non-Terrestrial Systems for 6G I [Room: Pisces 4] 2. Innovations in Computational Intelligence: Studies on Structures, Detection, & Optimization [Room: Virgo 1] 3. Novel Hardware Implementation of Learning Algorithms in Deep & Spiking Neural Networks II [Room: Virgo 2] 4. Delta-Sigma ADCs & its AI Application [Room: Virgo 3]	**Workshop/Other** 1. Climate Change Workshop [Room: Leo 1] 2. CASS Mentoring [Room: Virgo 4]	N/A
16:30-17:00	**Coffee Break**			**Poster/Demo/ Competition** 1. Poster (4 Sessions) 2. PhD Forum 3. Student Design Competition Demo [Room: Leo 2, 3, 4]
17:00-18:30	**Regular Sessions** 1. Analog Signal Processing I [Room: Aquarius 1] 2. Sigma Delta Modulator for ADC [Room: Aquarius 2] 3. Low Power Logic, Circuits & Architectures II [Room: Aquarius 3] 4. Digital Circuits, Systems & Architecture for Machine Learning II [Room: Aquarius 4] 5. Cryptography & Hardware Security [Room: Gemini 1] 6. Circuits & Systems for Wireless Power Transfer Applications [Room: Gemini 2] 7. Machine Learning & Signal Processing for Biomedical Systems I [Room: Pisces 1] 8. Neural Learning Systems: Techniques & Applications I [Room: Pisces 2] 9. Deep Learning for Visual Signal Representation & Processing [Room: Pisces 3]	**Special Sessions** 1. Optical & Wireless Communication & Sensing Technologies in Terrestrial & Non-Terrestrial Systems for 6G II [Room: Pisces 4] 2. Improving Student Retention & Use of AI/ChatGPT in Engineering Education [Room: Virgo 1] 3. Various Synchronization in Coupled Nonlinear Circuits with Specialized Coupling & Applications [Room: Virgo 2] 4. AI-Based Detection & Estimation for Health & Security Applications [Room: Virgo 3]	**Workshop/Other** 1. Climate Change Workshop [Room: Leo 1]	
18:30-21:00	**WiCAS-YPCAS Event** [Room: Leo 1]			

Time: UTC+8	Tuesday, May 21			
07:45-08:30	**Registration** [Foyer of Taurus Room (Secretariat Room)]			
08:30-10:00	**Regular Sessions** 1. Fractional N & All Digital PLL [Room: Aquarius 1] 2. ADC/DAC Circuits [Room: Aquarius 2] 3. Advanced Memory & Computing-in-Memory Circuits I [Room: Aquarius 3] 4. Digital Circuits, Systems & Architecture for Machine Learning III [Room: Aquarius 4] 5. Wireless Communications I [Room: Gemini 1] 6. Modelling & Control of Power & Energy Circuits & Systems [Room: Gemini 2] 7. Multimedia Systems for Coding & Processing [Room: Pisces 1] 8. Neuromorphic Spiking Learning Systems & Applications I [Room: Pisces 2]	**Special Sessions** 1. Compact Smart Wearable Devices & Digital Health [Room: Pisces 4] 2. Grand Challenge on Neural Network-based Video Coding [Room: Virgo 1] 3. Trustable & Sustainable Intelligent Circuits & System Design [Room: Virgo 3]	**Workshop/Other** 1. CASS Standards Association Workshop [Room: Virgo 4] 2. Info Security Workshop [Room: Leo 1] 3. ISCAS PhD Forum [Room: Pisces 3] 4. 12th International Workshop on Computational Intelligence for Multimedia Understanding [Room: Virgo 2]	**Poster/Demo** 1. Poster (12 Sessions) [Room: Leo 2, 3, 4]
10:00-10:30	**Coffee Break**			
10:30-11:30	**Keynote 4:** Hemanth Jagannathan, IBM Distinguished Engineer, Chiplet & Advanced Packaging Technology, IBM Research, USA [Venue: B2 Ballroom]			
11:30-12:30	**Keynote 5:** Michael Tse, Chair Professor of Electrical Engineering and Associate Vice President at City University of Hong Kong, Hong Kong [Venue: B2 Ballroom]			
12:30-13:30	**Lunch** [Venue: B2 Ballroom]			

Time: UTC+8	Tuesday, May 21 (Continue)			
13:30-14:00	**Award Ceremony** [Venue: Leo 1]			
14:00-14:30	**CASS 75th Anniversary** [Room: B2 Ballroom]			
14:30-15:30	**Past President Sharing Panel** [Room: Room: B2 Ballroom]			
15:30-16:00	**Coffee Break**			**Poster/Demo** 1. Poster (11 Sessions) 2. Live Demo II [Room: Leo 2, 3, 4]
16:00-17:30	**Regular Sessions** 1. High Frequency PLLs & Oscillators [Room: Aquarius 1] 2. ADC Circuit Techniques [Room: Aquarius 2] 3. Advanced Memory & Computing-in-Memory Circuits II [Room: Aquarius 3] 4. Digital Circuits, Systems & Architecture for Machine Learning IV [Room: Aquarius 4] 5. 6G, IoT Systems & Sensor Networks I [Room: Gemini 1] 6. High-Efficiency Power Converters & Drive Circuits [Room: Gemini 2] 7. Deep Learning in Multimedia Applications [Room: Pisces 1] 8. Neuromorphic Spiking Learning Systems & Applications II [Room: Pisces 2] 9. Signal Processing for Sensor Arrays & Networks [Room: Pisces 3]	**Special Sessions** 1. Emerging Technologies in Neural Prosthetic & Bio-inspired Devices [Room: Pisces 4] 2. Emerging Non-Volatile Devices for Computing [Room: Virgo 1] 3. Technology & Agribusiness [Room: Virgo 2] 4. Physical Hardware Evaluation from Design Trust to System Reliability [Room: Virgo 3]	**Workshop/Other** 1. CASS Standards Association Workshop [Room: Virgo 4] 2. Info Security Workshop [Room: Leo 1]	
19:00-22:00	**Gala Dinner** [Venue: B2 Ballroom]			

Time: UTC+8	Wednesday, May 22			
07:45-09:00	**Registration** [Foyer of Taurus Room (Secretariat Room)]			
09:00-10:30	**Regular Sessions** 1. Voltage Regulators & Current Reference [Room: Aquarius 1] 2. Memory Circuits & Interconnects [Room: Aquarius 2] 3. SOC, NOC, Multi-Core, & 3D/2.5D Systems [Room: Aquarius 3] 4. Circuit Techniques for Computing-in-Memory & Machine Learning [Room: Aquarius 4] 5. Quantum Computing Circuits & Systems I [Room: Gemini 1] 6. Education in Circuits & Systems I [Room: Gemini 2] 7. Biomedical Circuits & Systems I [Room: Pisces 1] 8. Neuromorphic Systems I [Room: Pisces 2] 9. Image Processing [Room: Pisces 3]	**Special Sessions** 1. Brain Computer Interface: Algorithm & Signal Processing [Room: Pisces 4] 2. Improving the Accuracy & Reliability of Analog-Based In-Memory Computing Systems I [Room: Virgo 1] 3. Smart 6G Wireless Baseband: Design & Implementations [Room: Virgo 2] 4. Efficient Processing of Large Language Models at the Edge [Room: Virgo 3]	**Workshop/Other** 1. AutoCAS Workshop [Room: Leo 1] 2. 3D Integration & Advanced Packaging Workshop [Room: Virgo 4]	N/A
10:30-11:00	**Coffee Break**			**Poster/Demo** 1. Poster (11 Sessions) 2. Live Demo III [Room: Leo 2, 3, 4]
11:00-12:30	**Regular Sessions** 1. Analog Techniques I [Room: Aquarius 1] 2. Voltage Reference Circuits [Room: Aquarius 2] 3. Programmable & Reconfigurable Array Architectures [Room: Aquarius 3] 4. Ultra-low Power Circuits & Systems [Room: Aquarius 4] 5. Advanced CMOS, Cryogenics and 3D Integration [Room: Gemini 1] 6. Dynamic & Event-Driven Vision Sensors [Room: Gemini 2] 7. Biomedical Circuits & Systems II [Room: Pisces 1] 8. Neuromorphic Systems II [Room: Pisces 2] 9. Filter Design, Implementation & Application [Room: Pisces 3]	**Special Sessions** 1. Brain Computer Interface: Hardware & Circuit Design [Room: Pisces 4] 2. Improving the Accuracy & Reliability of Analog-Based In-Memory Computing Systems II [Room: Virgo 1] 3. Recent Progress in Analysis & Estimation of Bifurcation Phenomena [Room: Virgo 2] 4. Ultra-Low-Power ICs Enabling Sensor Nodes Without Batteries [Room: Virgo 3]	**Workshop/Other** 1. AutoCAS Workshop [Room: Leo 1] 2. 3D Integration & Advanced Packaging Workshop [Room: Virgo 4]	
12:30-13:30	**Lunch** [Venue: B2 Ballroom]			

Time: UTC+8	Wednesday, May 22 (Continue)			
13:30-15:00	**Regular Sessions** 1. Photonics & mm-Wave Circuits [Room: Aquarius 1] 2. RF & mm-Wave Circuits I [Room: Aquarius 2] 3. Hardware Security for Logic, Circuits & Architectures I [Room: Aquarius 3] 4. Advanced Techniques for Digital Integrated Circuits & Systems I [Room: Aquarius 4] 5. Computing with Emergent Technologies II [Room: Gemini 1] 6. Sensory Signals Processing Circuits [Room: Gemini 2] 7. Wearable Biomedical Circuits & Systems I [Room: Pisces 1] 8. Neural Memristive In-Memory Computation Systems [Room: Pisces 2] 9. Machine Learning for Speech & Language Processing [Room: Pisces 3]	**Special Sessions** 1. Intelligent & Data Analytics to Real-Life Complex Networks & Nonlinear Systems I [Room: Pisces 4] 2. Artificial Intelligence in Power & Energy Circuits & Systems I [Room: Virgo 1] 3. Emerging AI-driven Visual Computing & Multimodal Learning for Real-world Applications [Room: Virgo 2] 4. Theory & Applications of Memristor Devices, Circuits, & Systems for Bio-Inspired Electronics I [Room: Virgo 3]	**Workshop/Other** 1. GeronCAS Workshop [Room: Leo 1]	N/A
15:00-15:30	**Coffee Break**			**Poster/Demo** 1. Poster (10 Sessions) [Room: Leo 2, 3, 4]
15:30-17:00	**Regular Sessions** 1. Analog Techniques II [Room: Aquarius 1] 2. Time Interleaved & SAR ADC [Room: Aquarius 2] 3. Hardware Security for Logic, Circuits & Architectures II [Room: Aquarius 3] 4. Electronic Design Automation & Physical Design I [Room: Aquarius 4] 5. Computing with Emergent Technologies I [Room: Gemini 1] 6. 2D/3D Image Sensors [Room: Gemini 2] 7. Lab-on-Chip & Point-of-Care Biomedical Diagnostics [Room: Pisces 1] 8. Biomedical Signal & Image Processing [Room: Pisces 3]	**Special Sessions** 1. Intelligent & Data Analytics to Real-Life Complex Networks & Nonlinear Systems II [Room: Pisces 4] 2. Millimeter-Wave & Sub-THz 5G/6G/SATCOM Broadband Circuits & Systems [Room: Virgo 1]	**Workshop/Other** 1. GeronCAS Workshop [Room: Leo 1]	
17:00-18:00	**Conference Awards & ISCAS 2025 Presentation** [Leo 1]			
18:30-21:00	**Farewell Reception** [Venue: Malaysian Food Street at Resorts World Sentosa]			

Technical Program: Sunday 19 May 2024

7:45 am – 8:30 am
Registration
Venue: Foyer of Taurus Room (Secretariat Room)

8:30 am – 5:00 pm
Tutorial: Mixed-Signal RF Transmitters
FULL DAY TUTORIAL
Venue: Pisces 2
Speakers: David J. Allstot, Vanessa Chen, Jeffrey S. Walling

8:30 am – 5:00 pm
Tutorial: Advanced Biomedical Imaging Technologies: Circuit Design and Techniques
FULL DAY TUTORIAL
Venue: Pisces 1
Speaker(s): Yuanjin Zheng, Yongfu Li, Jian Zhao, Ka-Meng Lei

8:30 am – 5:00 pm
Tutorial: Integrated Devices, Circuits and Systems for Quantum Computing
FULL DAY TUTORIAL
Venue: Leo 1
Speaker(s): Andreas Fuhrer Janett, Christian Enz, Andrei Vladimirescu, Fabio Sebastiano, Edoardo Charbon, Joseph Bardin, Sorin Voinigescu, Domenico Zito

8:30 am – 12:30 pm
Tutorial: More Efforts to Developing High-Performance PLLs with Jitter Reduction Approaching Sub-10fs
HALF DAY TUTORIAL
Venue: Aquarius 1
Speaker(s): Yong Chen (Nick)

8:30 am – 12:30 pm
Tutorial: Tensor Regression: Methods and Applications
HALF DAY TUTORIAL
Venue: Aquarius 2
Speaker(s): Yipeng Liu, Jiani Liu

8:30 am – 12:30 pm
Tutorial: Energy-Efficient AI-Native Wireless Communication Systems
HALF DAY TUTORIAL
Venue: Aquarius 3
Speaker(s): Rodney Martinez Alonso, Abdel Martinez Alonso

8:30 am – 12:30 pm
Tutorial: Advanced Mixed Signal Concepts and Circuit Innovations Exploiting Active Bulk-Driven Techniques using 22nm FD-SOI CMOS Technology (22FDX)
HALF DAY TUTORIAL
Venue: Aquarius 4
Speaker(s): Marcel Runge, Enne Wittenhagen, Friedel Gerfers

8:30 am – 12:30 pm
Tutorial: Using Neural Networks to Optimize the Design of Analog and Mixed-Signal Circuits and Systems
HALF DAY TUTORIAL
Venue: Gemini 1
Speaker(s): José M. de la Rosa

10:00 am – 10:30 am
Coffee Break
NETWORKING

12:30 pm – 1:30 pm
Lunch
NETWORKING
Venue: West Lobby, Foyer beside Aquarius 1

1:30 pm – 5:00 pm
Tutorial: How to Model the Training and Inference of Analog-Based In-Memory Computing (AIMC) Systems
HALF DAY TUTORIAL
Venue: Aquarius 2
Speaker(s): Corey Lammie, Manuel Le Gallo, Malte Rasch, Kaoutar El Maghraoui

1:30 pm – 5:00 pm
Tutorial: Machine Learning for Automated Physical Design
HALF DAY TUTORIAL
Venue: Aquarius 3
Speaker(s): Ioannis Savidis, Pratik Shrestha

1:30 pm – 5:00 pm
Tutorial: Towards Battery-free and Low-cost Distributed Sensor Node: from Novel IC Approaches to System-level Industrial Design
HALF DAY TUTORIAL
Venue: Aquarius 4
Speaker(s): Orazio Aiello, Roberto La Rosa

1:30 pm – 5:00 pm
Tutorial: Hardware Security for Biomedical Circuits and Systems
HALF DAY TUTORIAL
Venue: Gemini 1
Speaker(s): Ibrahim (Abe) M. Elfadel

1:30 pm – 5:00 pm
Tutorial: New Era of Artificial Intelligence: Unleashing the Power of Large Models in Visual Applications
HALF DAY TUTORIAL
Venue: Gemini 2
Speaker(s): Jiaying Liu, Wen-Huang Cheng, Shuai Yang

3:00 pm – 3:30 pm
Coffee Break
NETWORKING

3:00 pm – 4:00 pm
CASS Blitz ISCAS2024 Edition
SPECIAL EVENT
Venue: Aquarius 1
Session Chair(s): Santhosh Miriala (Anurag University), Alex James (Digital University Kerala)

6:00 pm – 9:00 pm
Welcome Reception
SOCIAL EVENT
Venue: Gardens By the Bay (Flower Field Hall and Water View Room)

Technical Program: Monday 20 May 2024

7:45 am – 8:30 am
Registration
Venue: Foyer of Taurus Room (Secretariat Room)

8:30 am – 9:00 am
Opening Ceremony
SPECIAL EVENT

Venue: B2 Ballroom

9:00 am – 10:00 am
Keynote: Towards Chips that Rewire Themselves? …How Novel Material-System Co-Design can enable them
KEYNOTE

Venue: B2 Ballroom
Speaker: Aaron Thean, Deputy President (Academic Affairs) and Provost, National University of Singapore, Singapore
Session Chair(s): Nam Ling (Santa Clara University, USA)

10:00 am – 11:00 am
Keynote: Moore with Less: Ultra-Low Energy Neuromorphic Circuits and Systems for Large-Scale Distributed AI
KEYNOTE

Venue: B2 Ballroom
Speaker: Gert Cauwenberghs, Professor, Co-Director of the Institute for Neural Computation, University of California San Diego, USA
Session Chair(s): Andrei Vladimirescu (University of California, Berkeley, USA)

11:00 am – 11:30 am
Coffee Break
NETWORKING

11:00 am – 1:00 pm
A1P-14 SAR ADC I
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Liheng Lou (University of Science and Technology of China)

ID1223: **A 27.5 fJ/Step SAR Capacitance-to-Digital Converter Based on Correlated Double Sampling**
Qingjiang Xia (Peking University, China), You You (Peking University, China), Yacong Zhang (Peking University, China), Wengao Lu (Peking University, China), Runkun Zhu (Peking University, China), Zhongjian Chen (Peking University, China)

ID1303: **A 91 dB SNDR Calibration-Free Fully-Passive Noise-Shaping SAR ADC with Mismatch Error Shaping**
Yu Lu (Fudan University, China), Hongwei Shen (Beijing Smart-Chip Microelectronics Technology Co. Ltd., China), Qingsong Zhang (Fudan University, China), Pengfei Jiang (Fudan University, China), Tianyue Sun (Fudan University, China) Yuxin Liao (Fudan University, China), Mengjiao Li (Beijing Smart-Chip Microelectronics Technology Co. Ltd., China), Hao Min (Fudan University, China)

ID1332: **A Simple Zero Average Switching Energy Differential SAR ADC**
Llorenç Fanals-I-Batllori (Universitat Politècnica de Catalunya, Spain), Namit Mishra (SLAC National Accelerator Laboratory, United States), Lorenzo Rota (SLAC National Accelerator Laboratory, United States), Aldo Pena-Perez (SLAC National Accelerator Laboratory, United States)

ID1380: **A Circuit-Generator-Aided Design Methodology for GHz Pipelined SAR ADCs**
Xingyu Lv (Tsinghua University, China), Rongyan Chen (South China University of Technology, China), Xian Tang (Tsinghua University, China)

ID2085: **A Self-Calibrated Sampling Noise Cancellation Technique for Noise-Shaping SAR ADC**
Zhengyuan Lou (Shanghai Jiao Tong University, China), Meng Xu (Shanghai Jiao Tong University, China), Yuekang Guo (Shanghai Jiao Tong University, China), Jing Jin (Shanghai Jiao Tong University, China), Jianjun Zhou (Shanghai Jiao Tong University, China)

11:00 am – 1:00 pm
A1P-15 SAR ADC II
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Ankesh Jain (IIT Delhi)

ID1207: **Loop Filter Design Considerations for Noise-Shaping in SAR ADCs**
Anamika Sharma (Indian Institute of Technology Bombay, India), Luv Pandey (STMicroelectronics, India), Paras Garg (STMicroelectronics, India), Rajesh Zele (Indian Institute of Technology Bombay, India)

ID1294: **A 105-dB SFDR 16-Bit SAR ADC with a Window Capacitor Calibration Scheme**
Qi-Fen Zeng (National Taiwan University of Science and Technology, Taiwan), Chia-Hui Tien (National Taiwan University of Science and Technology, Taiwan), Yung-Hui Chung (National Taiwan University of Science and Technology, Taiwan)

ID2262: **A 12-Bit 75 MS/s Asynchronous SAR ADC with Gain-Boosting Dynamic Comparator**
Renhe Chen (ShanghaiTech University, China), Albert Lee (Inston Tech, China), Yongqi Hu (ShanghaiTech University, China), Hao Xu (Fudan University, China), Xufeng Kou (ShanghaiTech University, China)

ID2265: **A 10-Bit 100 kS/s SAR ADC with a Monotonic Capacitor Switching Procedure for Single-Ended Inputs in 22 nm CMOS FDSOI**
Alexander Meyer (Technische Universität Braunschweig, Germany), Kaoru Yamashita (Keio University, Japan), Adilet Dossanov (Technische Universität Braunschweig, Germany), Martin Maier (Technische Universität Braunschweig, Germany), Finn Stapelfeldt (Technische Universität Braunschweig, Germany) Yerzhan Kudabay (Technische Universität Braunschweig, Germany), Peter Toth (Technische Universität Braunschweig, Germany), Fa Foster Dai (Auburn University,

United States), Hiroki Ishikuro (Keio University, Japan), Vadim Issakov (Technische Universität Braunschweig, Germany)

ID2538: **Reinforcement-Learning-Based Successive Approximation Algorithm**
Hamed Nasiri (Memorial University of Newfoundland, Canada), Cheng Li (Memorial University of Newfoundland, Canada), Lihong Zhang (Memorial University of Newfoundland, Canada)

11:00 am – 1:00 pm
A1P-16 Hardware Security for IoT, Circuits, & Cyber-Physical Systems II
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Chip Hong Chang (Nanyang Technological University)

ID1366: **3881 Gbps/W, 3005 μm² AES Core with State Based Clock Gating for IoT Applications**
Zhangyi Pei (Nanyang Technological University, Singapore), Vishnu Paramasivam Nambiar (Institute of Microelectronics, Agency for Science, Technology and Research, Singapore), Yi Sheng Chong (Institute of Microelectronics, Agency for Science, Technology and Research, Singapore), Wang Ling Goh (Nanyang Technological University, Singapore), Anh Tuan Do (Institute of Microelectronics, Agency for Science, Technology and Research, Singapore)

ID1696: **Optimisation of RO-PUF Design Parameters for Minimising the Effective Area Per PUF Bit**
Björn Driemeyer (Universität Ulm, Germany), Holger Mandry (Universität Ulm, Germany), David-Peter Wiens (Universität Ulm, Germany), Joachim Becker (Universität Ulm, Germany), Maurits Ortmanns (Universität Ulm, Germany)

ID2004: **Enhancing Identifiability of PUFs with Built-In Compensation Through Nonlinear Transformations**
Raúl Aparicio-Téllez (Universidad de Zaragoza, Spain), Miguel Garcia-Bosque (Universidad de Zaragoza, Spain), Guillermo Díez-Señorans (Universidad de Zaragoza, Spain), Santiago Celma (Universidad de Zaragoza, Spain)

ID2339: **Fortifying Strong PUFs: A Modeling Attack-Resilient Approach Using Weak PUF for IoT Device Security**
Sara Alahmadi (University of Louisiana at Lafayette, United States), Kasem Khalil (University of Mississippi, United States), Haytham Idriss (University Fort Wayne, United States), Magdy Bayoumi (University of Louisiana at Lafayette, United States)

11:00 am – 1:00 pm
A1P-17 Hardware Security for IoT, Circuits, & Cyber-Physical Systems III
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Yeong-Kang Lai (National Chung Hsing University)

ID1129: **Highly Reliable PUF Circuits Using Efficient Post-Processing Stabilization Technique**
Yu-Hsiang Tseng (National Taiwan University, Taiwan), Shao-Hong Yang (National Taiwan University, Taiwan), Tsung-Te Liu (National Taiwan University, Taiwan)

ID1152: **A Novel Methodology for Processor Based PUF in Approximate Computing**

Aditya Japa (Queen's University Belfast, United Kingdom), Jack Miskelly (Queen's University Belfast, United Kingdom), Yijun Cui (Nanjing University of Aeronautics and Astronautics, China), Máire O'Neill (Queen's University Belfast, United Kingdom), Chongyan Gu (Queen's University Belfast, United Kingdom)

ID1382: An SRAM-Based PUF with Noise Immunity Achieving 0.58% Native BER in 55-nm CMOS
Zexin Su (University of the Chinese Academy of Sciences, China), Bo Li (Institute of Microelectronics Chinese Academy of Sciences, China), Chang Liu (Institute of Microelectronics Chinese Academy of Sciences, China), Xiaohui Su (Institute of Microelectronics Chinese Academy of Sciences, China), Qian Luo (Institute of Microelectronics Chinese Academy of Sciences, China), Hongyu Ren (Institute of Microelectronics Chinese Academy of Sciences, China), Zhengsheng Han (Institute of Microelectronics Chinese Academy of Sciences, China)

ID1775: Enhancing Circuit Authentication Through Secure Isolation
Kais Belwafi (Khalifa University, U.A.E.), Hamdan Alshamsi (Khalifa University, U.A.E.), Ashfaq Ahmed (Khalifa University, U.A.E.), Abdulhadi Shoufan (Khalifa University, U.A.E.)

ID2553: A Unified OTP and PUF Exploiting Post-Program Current on Standard CMOS Technology
Ronaldo Serrano (University of Electro-Communications, Japan), Ckristian Duran (University of Tokyo, Japan), Marco Sarmiento (University of Electro-Communications, Japan), Khai-Duy Nguyen (University of Electro-Communications, Japan), Tetsuya Iizuka (University of Tokyo, Japan), Trong-Thuc Hoang (University of Electro-Communications, Japan), Cong-Kha Pham (University of Electro-Communications, Japan)

11:00 am – 1:00 pm
A1P-18 Computing with Emergent Technologies III
TRACK 5: BEYOND CMOS: NANOELECTRONICS AND HYBRID SYSTEMS INTEGRATION

Venue: Leo 2+3+4
POSTER
Session Chair(s): Vasileios Ntinas (TU Dresden)

ID1385: An Integration and Time-Sampling Based Readout Circuit with Current Compensation for Parallel MAC Operations in RRAM Arrays
Weiping Yang (National University of Defense Technology, China), Shilin Zhou (National University of Defense Technology, China), Hui Xu (National University of Defense Technology, China), Qimin Zhou (National University of Defense Technology, China), Jingyu Li (National University of Defense Technology, China), Qingjiang Li (National University of Defense Technology, China), Yinan Wang (National University of Defense Technology, China), Changlin Chen (National University of Defense Technology, China)

ID2061: Single Slope ADC with Reset Counting for FeFET-Based In-Memory Computing
Nellie Laleni (Fraunhofer Institute for Photonic Microsystems IPMS; ETH Zürich, Germany), Sahana Padma (Fraunhofer Institute for Photonic Microsystems IPMS, Germany), Thomas Kämpfe (Fraunhofer Institute for Photonic Microsystems IPMS, Germany), Taekwang Jang (ETH Zürich, Switzerland)

ID2256: High-Speed Serial and Semi-Parallel IMPLY-Based Approximate Adders Through Memristors for In-Memory Computing
Nandit Kaushik (Indian Institute of Technology Mandi, India), Hemanth L Krishna (Indian Institute of Technology Mandi, India), Srinivasu Bodapati (Indian Institute of Technology Mandi, India)

ID2548: A Closed-Loop Readout Circuit with Voltage Drop Mitigation for Emerging Resistive Technologies
Andrea Mifsud (Imperial College London, United Kingdom), Adil Malik (Imperial College London, United Kingdom), Abdulaziz Alshaya (Imperial College London, United Kingdom), Peilong Feng (Imperial College London, United Kingdom), Timothy G. Constandinou (Imperial College London, United Kingdom)

ID2591: HXNOR-PBNN: A Scalable and Parallel Spintronics Synaptic Architecture for Probabilistic Binary Neural Networks
Cancheng Xiao (Tsinghua University, China), Yuxuan Ma (Tsinghua University, China), Dingsong Jiang (Tsinghua University, China), Jianle Liu (Tsinghua University, China), Bingqian Song (Tsinghua University, China), Jianshi Tang (Tsinghua University, China), Huaqiang Wu (Tsinghua University, China), Tianxiang Nan (Tsinghua University, China)

11:00 am – 1:00 pm
A1P-19 Advanced Technologies for Front-end & Back-end-of-line
TRACK 5: BEYOND CMOS: NANOELECTRONICS AND HYBRID SYSTEMS INTEGRATION

Venue: Leo 2+3+4
POSTER
Session Chair(s): Vita Pi-Ho Hu (National Taiwan University)

ID1010: Modeling and Analysis of Waferscale Switching Network with Multiple System Faults
Zhiquan Wan (Zhejiang Lab, China), Zhipeng Cao (People's Liberation Army Strategic Support Force Information Engineering University, China), Shunbin Li (Zhejiang Lab, China), Dehao Ye (Zhejiang Lab, China)

ID2048: Nanoelectromechanical Analog-to-Digital Converter for Low Power and Harsh Environments
Elliott Worsey (University of Bristol, United Kingdom), Qi Tang (University of Bristol, United Kingdom), Manu Bala Krishnan (University of Bristol, United Kingdom), Mukesh Kumar Kulsreshath (University of Bristol, United Kingdom), Dinesh Pamunuwa (University of Bristol, United Kingdom)

ID2124: A VCO-Based Readout ADC for Quasi-Static Sensing Applications in 3-μm Low-Temperature Poly-Silicon Thin-Film Transistor Technology
Chia-Hsiang Chang (National Taiwan University, Taiwan), Pang-Cheng Chen (National Taiwan University, Taiwan), Hsiang-Chi Cheng (AUO Corporation, Taiwan), Chung-Hung Chen (AUO Corporation, Taiwan), Chun-Yen Lin (National Taiwan University, Taiwan), Chih-Ting Lin (National Taiwan University, Taiwan), Tsung-Hsien Lin (National Taiwan University, Taiwan)

ID2276: Negative Capacitance FET 8T SRAM Computing In-Memory Based Logic Design for Energy Efficient AI Edge Devices
Venu Birudu (SRM University AP, India), Tirumala Rao Kadiyam (SRM University AP, India), Koteswara Rao Penumalli (SRM University AP, India), Aditya Japa (Queen's University Belfast, United Kingdom), Sushma Sambatur (Global Foundries, India), Chongyan Gu (Queen's University Belfast, United Kingdom), Siva Sankar Yellampalli (SRM University AP, India), Ramesh Vaddi (SRM University AP, India)

ID2284: Impact of S/D Extension Length and Sheet Stacking on Transient Behavior of Nanosheet FETs
Shobhit Srivastava (Sardar Vallabhbhai National Institute of Technology, India), Sachin Doge (Sardar Vallabhbhai National Institute of Technology, India), Sourabh Panwar (Sardar Vallabhbhai National Institute of Technology, India), Shashidhara M (Sardar Vallabhbhai National Institute of Technology & People's Education Society University, India), Vivek Garg (Sardar Vallabhbhai

National Institute of Technology, India), Shivendra Yadav (Sardar Vallabhbhai National Institute of Technology, India), Lomash Chandra (Indian Institute of Technology Roorkee, India), Abhishek Acharya (Sardar Vallabhbhai National Institute of Technology, India)

ID1029: **Assessing the Performance of Stateful Logic in 1-Selector-1-RRAM Crossbar Arrays**Arjun Tyagi (Technion - Israel Institute of Technology, Israel), Shahar Kvatinsky (Technion - Israel Institute of Technology, Israel)

ID1899: **Interface Trap Analysis in Multi-Fin FinFET Technology: A Crucial Reliability Issue in Digital Application**
Jyoti Patel (Indian Institute of Technology Roorkee, India), Sankalp Rai (Graphic Era University, India), Vivek Kumar (National Institute of Technology, Uttarakhand, India), Sudeb Dasgupta (Indian Institute of Technology Roorkee, India)

11:00 am – 1:00 pm
A1P-20 Biomedical Circuits & Systems
TRACK 6: BIOMEDICAL CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Jennifer Blain Christen (Arizona State university, Tempe, AZ, USA)

ID1517: **A 0.816nW 12.3pS Tunable Low-Gm Transconductor for Bio-Electrical Signal Acquisition**
Feng Yan (Sun Yat-sen University, China), Bingjun Xiong (Sun Yat-sen University, China), Wenji Mo (Sun Yat-sen University, China), Kangkang Sun (Sun Yat-sen University, China), Jian Guan (Sun Yat-sen University, China), Jingjing Liu (Sun Yat-sen University, China)

ID1576: **A Charge-Balanced Monopolar Neural Stimulator by Utilizing Dynamic Current Replication Technique Achieving <1 nA Residual Average DC Current Error**
Jianye Li (Tianjin University, China), Jialei Wu (Tianjin University, China), Yixin Zhou (Southeast University, China), Keping Wang (Tianjin University, China)

ID2168: **Reducing Power Consumption in LNA by Utilizing EEG Signals as Basis Matrix in Compressed Sensing**
Riku Matsubara (Osaka University, Japan), Daisuke Kanemoto (Osaka University, Japan), Tetsuya Hirose (Osaka University, Japan)

ID2568: **A 140-dB Dynamic Range Digital PPG Front-End IC with an Integrated MoSe2 Photodiode for Wearable Non-Invasive Pulse Oximetry**
Yu Liu (University of Electronic Science and Technology of China/Chengdu Transepic Semiconductor Co.,Ltd., China), Chao Chen (Zhejiang University, China), Yixuan Huang (University of Electronic Science and Technology of China, China), Qiao He (University of Electronic Science and Technology of China, China), Jiang Wu (University of Electronic Science and Technology of China, China)

ID1683: **A 199 µW, 82.9% Efficiency Current Driver with Active Common-Mode Reduction for Impedance-Based Tactile Sensors**
Zhentao Wu (University College London, United Kingdom), Yu Wu (University College London, United Kingdom), Andreas Demosthenous (University College London, United Kingdom)

ID2263: **FPGA-Based Hardware Software Co-Design to Accelerate Brain Tumour Segmentation**

Vinay Rayapati (International Institute of Information Technology Bangalore, India), Ravi Kiran Reddy Gogireddy (International Institute of Information Technology Bangalore, India), Ajay Kumar Gandi (International Institute of Information Technology Bangalore, India), Saketh Gajawada (International Institute of Information Technology Bangalore, India), Gopala Krishna Reddy Sanampudi (International Institute of Information Technology Bangalore, India), Nanditha Rao (International Institute of Information Technology Bangalore, India)

ID2308: Signal Analysis and Detection of COVID-19 Infection with ATR-FTIR Spectroscopy
Yina Li (Nanyang Technological University, Singapore), Wenwen Zhang (Nanyang Technological University, Singapore), Zhouzhuo Tang (Beihang University, China), Yingmei Feng (Capital Medical University, China), Xia Yu (Beihang University, China), Qijie Wang (Nanyang Technological University, Singapore), Zhiping Lin (Nanyang Technological University, Singapore)

11:00 am – 1:00 pm
A1P-21 Neural Learning Systems: Techniques & Applications II
TRACK 8: NEURAL NETWORKS AND NEUROMORPHIC ENGINEERING

Venue: Leo 2+3+4
POSTER
Session Chair(s): Zhuo Zou (Fudan University)

ID1137: i6mA-CNN: A Web-Based System to Identify DNA N⁶-Methyladenine Sites in Mouse Genomes
Thanh-Hoang Nguyen-Vo (Victoria University of Wellington, New Zealand), Susanto Rahardja (Northwestern Polytechnical University & Singapore Institute of Technology, Singapore), Binh Nguyen (Victoria University of Wellington, New Zealand)

ID1798: Compensation Architecture to Alleviate Noise Effects in RRAM-Based Computing-in-Memory Chips with Residual Resource
Xiaoqing Zhao (Xi'an Jiaotong University, China), Longjun Liu (Xi'an Jiaotong University, China), Yuyi Liu (Beijing Innovation Center for Future Chips, Tsinghua University, China), Bin Gao (Beijing Innovation Center for Future Chips, Tsinghua University, China), Hongbin Sun (Xi'an Jiaotong University, China)

ID2173: BITLITE: Light Bit-Wise Operative Vector Matrix Multiplication for Low-Resolution Platforms
Vince Tran (University of Toronto, Canada), Demeng Chen (University of Toronto, Canada), Roman Genov (University of Toronto, Canada), Mostafa Rahimi Azghadi (James Cook University, Australia), Amirali Amirsoleimani (York University, Canada)

ID2391: KARS: Kernel-Grouping Aided Row-Skipping for SDK-Based Weight Compression in PIM Arrays
Juhong Park (Sungkyunkwan University, Korea), Johnny Rhe (Sungkyunkwan University, Korea), Jong Hwan Ko (Sungkyunkwan University, Korea)

ID1848: Dynamic Gradient Sparse Update for Edge Training
I-Hsuan Li (National Yang Ming Chiao Tung University, Taiwan), Tian Sheuan Chang (National Yang Ming Chiao Tung University, Taiwan)

ID1258: A Ready-to-Use RTL Generator for Systolic Tensor Arrays and Analysis Using Open-Source EDA Tools
Jooyeon Lee (Daegu Gyeongbuk Institute of Science and Technology, Korea), Donghun Lee (Chungnam National University, Korea), Jaeha Kung (Korea University, Korea)

ID1705: Reducing the Energy Dissipation of Large Language Models (LLMs) with Approximate Memories
Zhen Gao (Tianjin University, China), Jie Deng (Tianjin University, China), Pedro Reviriego (Universidad Politécnica de Madrid, Spain), Shanshan Liu (University of Electronic Science and Technology of China, China), Fabrizio Lombardi (Northeastern University, United States)

11:00 am – 1:00 pm
A1P-22 Detection & Estimation
TRACK 10: DIGITAL SIGNAL PROCESSING

Venue: Leo 2+3+4
POSTER
Session Chair(s): Zhiping Lin (Nanyang Technological University)

ID1412: Learning-Based Human Detection via Radar for Dynamic and Cluttered Indoor Environments
Jiarui Zhang (Nanyang Technological University, Singapore), Songnan Lin (Nanyang Technological University, Singapore), Hao Cheng (Nanyang Technological University, Singapore), Weixian Liu (Nanyang Technological University, Singapore), Bihan Wen (Nanyang Technological University, Singapore)

ID1946: A Dual-Slope BlueFMCW Radar for Simultaneous Mitigation Against Close-In DRFM and Frequency Domain Spoofing Attacks
Soham Lakhote (Indian Institute of Science, India), Easha Easha (Indian Institute of Science, India), Gaurab Banerjee (Indian Institute of Science, India)

ID2474: Moving Object Detection in Shallow Underwater Using Multi-Scale Spatial-Temporal Lacunarity
Shaofeng Zou (Tsinghua University, China), Xuyang Wang (Tsinghua University, China), Tao Yuan (Tsinghua University, China), Kaihui Zeng (Tsinghua University, China), Guolin Li (Tsinghua University, China), Xiang Xie (Tsinghua University, China)

ID2286: A Method for Out-of-Distribution Detection in Encrypted Mobile Traffic Classification
Yuzhou Tong (Nanyang Technological University, Singapore), Yongming Chen (Nanyang Technological University, Singapore), Bah-Hwee Gwee (Nanyang Technological University, Singapore), Qi Cao (University of Glasgow Singapore, Singapore), Sirajudeen Gulam Razul (Nanyang Technological University, Singapore), Zhiping Lin (Nanyang Technological University, Singapore)

ID2249: Feature Map Guided Adapter Network for Object Detection in Low-Light Conditions
Cong Pang (ShanghaiTech University, China), Wei Zhou (ShanghaiTech University, China), Haoyan Li (ShanghaiTech University, China), Xiangyu Zhang (ShanghaiTech University, China), Xin Lou (ShanghaiTech University, China)

11:00 am – 1:00 pm
A1P-23 Live Demo I
TRACK 15: LIVE DEMO

Venue: Leo 2+3+4
POSTER
Session Chair(s): Chao Wang (Huazhong University of Science and Technology), Deruo Cheng (Nanyang Technological University)

ID1367: Live Demonstration: A Target-Separable BWN Inspired Speech Recognition Processor with Low-Power Precision-Adaptive Approximate Computing
Chenjie Xia (Southeast University, China), Xuanhao Zhang (Southeast University, China), Zihan Zou (Southeast University, China), Hao Cai (Southeast University, China), Bo Liu (Southeast University, China)

ID1620: Live Demonstration: A Low-Cost Wearable Continuous Monitoring Platform for Dengue
Xin Wang (Imperial College London, United Kingdom), Khayle Torres (Imperial College London, United Kingdom), Yuting Xu (Imperial College London, United Kingdom), Stefan Karolcik (Imperial College London, United Kingdom), Damien Ming (Imperial College London, United Kingdom), Sophie Yacoub (Oxford University Clinical Research Unit, Vietnam), Alison Holmes (Imperial College London, United Kingdom), Pantelis Georgiou (Imperial College London, United Kingdom)

ID2044: Live Demonstration: A Wearable Eight-Channel A-Mode Ultrasound System for Hand Gesture Recognition and Interactive Gaming
Yaohua Zhang (University College London, United Kingdom), Bruno Grandi Sgambato (Imperial College London, United Kingdom), Jiaxing Zhang (University College London, United Kingdom), Anette Jakob (Fraunhofer Institute for Biomedical Engineering IBMT, Germany), Marc Fournelle (Fraunhofer Institute for Biomedical Engineering IBMT, Germany), Mohamad Rahal (University College London, United Kingdom), Meng-Xing Tang (Imperial College London, United Kingdom), Dario Farina (Imperial College London, United Kingdom), Dai Jiang (University College London, United Kingdom), Andreas Demosthenous (University College London, United Kingdom)

ID2317: Live Demonstration: Real-Time Object Detection & Classification System in IoT with Dynamic Neuromorphic Vision Sensors
Zehao Li (Nanyang Technological University, Singapore), Wenhao Lu (Nanyang Technological University, Singapore), Yuncheng Lu (Nanyang Technological University, Singapore), Junying Li (Nanyang Technological University, Singapore), Yucen Shi (Nanyang Technological University, Singapore), Yuanjin Zheng (Nanyang Technological University, Singapore), Tony Tae-Hyoung Kim (Nanyang Technological University, Singapore)

ID2485: Live Demonstration: A Wearable Cardiopulmonary Healthcare System for Real-Term Monitoring of Multi-Modal Physiological Signals
Changyan Chen (Shanghai Jiao Tong University, China), Rui Pan (Shanghai Jiao Tong University, China), Huajie Huang (Shanghai Jiao Tong University, China), Xuya Jiang (Jiangnan University, China), Qing Zhang (Shanghai Jiao Tong University, China), Yuhang Zhang (Shanghai Jiao Tong University, China), Jian Zhao (Shanghai Jiao Tong University, China), Yongfu Li (Shanghai Jiao Tong University, China)

ID1177: Live Demonstration: 5-Bit Signed SRAM-Based DNN CIM for Image Recognition
Oscar Pereira-Rial (Universidade de Santiago de Compostela, Spain), Daniel García-Lesta (Universidade de Santiago de Compostela, Spain), Lorenzo Vaquero (Universidade de Santiago de Compostela, Spain), Paula López (Universidade de Santiago de Compostela, Spain), Victor Brea (Universidade de Santiago de Compostela, Spain), Diego Cabello (Universidade de Santiago de Compostela, Spain)

ID2043: Live Demonstration: Optical Communications Using Solar Cells
Walter Leon-Salas (Purdue University, United States), Diana Narvaez-Bernal (Purdue University, United States), Rodrigo Esparza (Tecnologico de Monterrey, Mexico), Gabriel Baquero (University of Houston, United States)

11:00 am – 1:00 pm
A1P-24 IoT Sensors
TRACK 7: SENSORY CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Jie Chen (University of Alberta, Edmonton, AB, Canada), Jennifer Blain Christen (Arizona State university, Tempe, AZ, USA)

ID1499: A 0.002-mm², 2.9-μW Pulse-Frequency-Modulation Based Temperature Sensor with 40-mK Resolution
Chiyuan Zhang (Kunming Institute of Physics, China), Nan Chen (Kunming Institute of Physics, China), Douming Hu (Kunming Institute of Physics, China), Fang Zhu (Kunming Institute of Physics, China), Yuesheng Pu (Kunming Institute of Physics, China), Libin Yao (Kunming Institute of Physics, China)

ID1701: Novel High Frequency Antenna Sensor to Detect On-Line Partial Discharge Signals
Yange Wang (Nanyang Technological University, Singapore), Wensong Wang (Nanyang Technological University, Singapore), Zhou Shu (National University of Singapore, Singapore), Yanshu Guo (Nanyang Technological University, Singapore), Shiquan Wang (Nanyang Technological University, Singapore), Yuanjin Zheng (Nanyang Technological University, Singapore)

ID2064: A Battery-Free and Sensor-Less Photovoltaic Tag for Real-Time Indoor Light Illuminance Evaluation
Cheng Tian (ShanghaiTech University, China), Zijie Chen (ShanghaiTech University, China), Junrui Liang (ShanghaiTech University, China)

ID2313: A Lossless Compression Algorithm with Hardware Implementation for Dynamic Vision Sensor
Zewei Ding (Fudan University, China), Shangmei Wang (Fudan University, China), Yujie Cai (Fudan University, China), Xiaoyang Zeng (Fudan University, China), Wenhong Li (Fudan University, China), Mingyu Wang (Fudan University, China)

ID2060: An Energy-Autonomous and Battery-Free Resistive Sensor Using a Time-Domain to Digital Conversion with Bluetooth Low Energy Connectivity
Mario Costanza (FEMTO-ST Institute, University of Franche-Comté, France), Antonino Pagano (University of Palermo, Italy), Samuel Margueron (FEMTO-ST Institute, University of Franche-Comté, France), Ilenia Tinnirello (University of Palermo, Consorzio Nazionale Interuniversitario per le Telecomunicazioni, Italy), Roberto La Rosa (STMicroelectronics, Italy)

ID2408: A 36nW Ultra-Wideband Wake-Up Receiver with -86dBm Sensitivity and Addressing Capabilities
Federico Villani (ETH Zürich, Switzerland), Enea Masina (ETH Zürich, Switzerland), Thomas Burger (ETH Zürich, Switzerland), Michele Magno (ETH Zürich, Switzerland)

11:00 am – 1:00 pm
A1P-25 Biomedical Sensors
TRACK 7: SENSORY CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Milin Zhang (Tsinghua University, Beijing, China), Yuanqi Hu (Beihang University, China)

ID1570: **Design of a Multi-Channel High-Sensitivity Electrochemical Interface IC Based on Organic Electrochemical Transistors (OECT)**
Yuan Ma (Tsinghua University, China), Shangbin Liu (Tsinghua University, China), Chao Xie (Tsinghua University, China), Yahao Song (Tsinghua University, China), Lan Yin (Tsinghua University, China), Milin Zhang (Tsinghua University, China)

ID1611: **All-Digital High-Resolution Frequency Measurement SoC for Rapid MEMS Readouts**
Hitesh Kumar Sahu (Indian Institute of Technology Bombay, India), Emon Sarkar (Indian Institute of Technology Bombay, India), Pushkar Sathe (Indian Institute of Technology Bombay, India), Laxmeesha Somappa (Indian Institute of Technology Bombay, India)

ID1734: **Miniaturized and Integrated On-Chip Ag/AgCl Micro-Electrodes for Chemical Detection**
Jing Liang (Beihang University, China), Xiaotao Jia (Beihang University, China), Yuanqi Hu (Beihang University, China)

ID1934: **Development and Evaluation of an IoT-Driven Auto-Infusion System with Advanced Monitoring and Alarm Functionalities**
Chiang Liang Kok (University of Newcastle Australia, Singapore), Tee Hui Teo (Singapore University of Technology and Design, Singapore), Yit Yan Koh (University of Newcastle Australia, Singapore), Yuwei Dai (University of Newcastle Australia, Singapore), Boon Kang Ang (University of Newcastle Australia, Singapore), Jian Ping Chai (University of Newcastle Australia, Singapore)

ID2210: **0.5V 32nW Inverter-Based Gm-C Filter for Bio-Signal Processing**
Ali Namdari (Università di Genova, Italy), Orazio Aiello (Università di Genova, Italy), Daniele D. Caviglia (Università di Genova, Italy)

11:30 am – 1:00 pm
Student Design Competition
SPECIAL EVENT

Venue: Leo 1
SPECIAL EVENT
Session Chair(s): Kea-Tiong (Samuel) Tang (National Tsing Hua University, Taiwan), Elisabetta Moisello (University of Pavia)

11:30 am – 1:00 pm
A2L-01 Amplifiers
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Aquarius 1
ORAL
Session Chair(s): Zunsong Yang (Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China.), Xinsheng Wang (Harbin Institute of Technology)

11:30 am
ID1363: **A Floating-Ring Hybrid Amplifier Insensitive to PVT and Common-Mode Variation Without CMFB for High-Speed ADCs**
Yaning Wang (Tsinghua University, China), Zhenguo Li (Beijing Smart-Chip Microelectronics Technology Co. Ltd., China), Peng Wang (Tsinghua University, China), Yihang Cheng (Tsinghua University, China), Fule Li (Tsinghua University, China), Yi Hu (Beijing Smart-Chip Microelectronics Technology Co. Ltd., China), Jiali Hou (Beijing Smart-Chip Microelectronics Technology Co. Ltd.,

China), Meng Su (Beijing Smart-Chip Microelectronics Technology Co. Ltd., China), Mengjiao Li (Beijing Smart-Chip Microelectronics Technology Co. Ltd., China)

11:48 am
ID2148: **A PVT-Robust Open-Loop Gm-Ratio ×16 Gain Residue Amplifier for >1 GS/s Pipelined ADCs**
Diogo André Dias (NOVA School of Science and Technology, Portugal), Tiago Costa (Delft University of Technology, Netherlands), João Goes (NOVA School of Science and Technology, Portugal)

12:06 pm
ID1641: **Design of a Linearized Power-Efficient Dynamic Amplifier in 22nm FDSOI**
Bangda Yang (University of Toronto, Canada), Tony Chan Carusone (University of Toronto, Canada)

12:24 pm
ID1452: **A 2.1/5.2-NEF/PEF Capacitively Coupled Instrumentation Amplifier with Fast -Settling for Biosensor**
Junwen Zhang (Zhejiang University, China), Xiaopeng Yu (Zhejiang University, China), Zhenghao Lu (Soochow University, China), Nick Nianxiong Tan (Zhejiang University, China), Xinjie Wu (Zhejiang University, China), Chenxu Jiang (Zhejiang University, China), Haowei Lu (Zhejiang University, China), Zhong Tang (Vango Technologies, Inc., China)

12:42 pm
ID2133: **High-CMRR, Operational Transconductance Amplifier for Low-Voltage Applications Based on a Degenerative Current TRAM**
Majid Radman (York University, Canada), Amir Sodagar (York University, Canada)

11:30 am – 1:00 pm
A2L-02 Models & Methods for Non-Linear Circuits & Systems
TRACK 9: METHODS AND MODELS FOR THE ANALYSIS/DESIGN OF NONLINEAR CIRCUITS AND SYSTEMS

Venue: Aquarius 2
ORAL
Session Chair(s): Federico Bizzarri (Politecnico di Milano-Italy), Maciej Ogorzałek (Jagiellonian University, Poland)

11:30 am
ID1076: **An Active-Perturbation Method to Estimate Online Inertia and Damping in Electric Power Systems**
Federico Bizzarri (Politecnico di Milano, Italy), Angelo Maurizio Brambilla (Politecnico di Milano, Italy), Davide Del Giudice (Politecnico di Milano, Italy), Daniele Linaro (Politecnico di Milano, Italy)

11:48 am
ID2387: **Fast Decoupling Capacitor Optimization for Power Delivery Network Based on Model and Data Fusion Method**
Jie Zheng (University of Electronic Science and Technology of China, China), Jienan Chen (University of Electronic Science and Technology of China, China), Peizhi Lei (University of Electronic Science and Technology of China, China), Zhaoting Ou (University of Electronic Science and Technology of China, China), Zeyan Lu (University of Electronic Science and Technology of China, China)

12:06 pm
ID1206: **A Nonlinear Model of Air-Gapped Ferrite-Core Inductors for SMPS Applications**

Alessandro Ravera (Università di Genova, Italy), Andrea Formentini (Università di Genova, Italy), Matteo Lodi (Università di Genova, Italy), Alberto Oliveri (Università di Genova, Italy), Marco Storace (Università di Genova, Italy)

12:24 pm
ID2198: **A Write System for Compact RRAM Memory Arrays Based on F-1T1R**
Michele Caselli (University of Parma, Italy), Andrea Boni (University of Parma, Italy)

12:42 pm
ID1041: **Comparison of DTC Segmentation Methods in Fractional-N Frequency Synthesizers**
Xu Wang (University College Dublin, Ireland), Michael Peter Kennedy (University College Dublin, Ireland)

11:30 am – 1:00 pm
A2L-03 Data Path & Arithmetic Circuits and Systems
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Aquarius 3
ORAL
Session Chair(s): Chung-An Shen (National Taiwan University of Science), Lan-Da Van (National Yang Ming Chiao Tung University)

11:30 am
ID1796: **Comprehensive Analysis of Input Order Invariant Approximate 4-2 Compressors for Binary Multipliers**
Ettore Napoli (University of Salerno, Italy), Antonio G.M. Strollo (University of Napoli Federico II, Italy), Efstratios Zacharelos (University of Salerno, Italy), Gennaro Di Meo (University of Napoli Federico II, Italy)

11:48 am
ID1887: **Mantissa-Aware Floating-Point Eight-Term Fused Dot Product Unit**
Wen Wang (Zhejiang University, China), Bingjie Xia (Zhejiang University, China), Bing Xiong (Zhejiang Lab, China), Xiaoxia Han (Zhejiang University, China), Peng Liu (Zhejiang Lab, Zhejiang University, China)

12:06 pm
ID1073: **An Optimized Architecture for Computing the Square Root of Complex Numbers**
Yu Wang (Nanjing Xiaozhuang University, China), Haoyu Zhang (Jinling Institute of Technology, China), Wei Hu (Jinling Institute of Technology, China), Xin Zhang (Jinling Institute of Technology, China), Xinyu Tian (Jinling Institute of Technology, China), Fei Lyu (Jinling Institute of Technology, China), Yuanyong Luo (Linx Lab, HiSilicon, Huawei Corporation, China)

12:24 pm
ID1699: **A Wide Range 2-to-2048 Division Ratio Frequency Divider Using 40-nm CMOS Process**
Soumika Majumder (National Sun Yat-sen University, Taiwan), Venkata Kolakaluri (National Sun Yat-sen University, India), Oliver Jose (National Sun Yat-sen University & Batangas State University, Philippines), Chua-Chin Wang (National Sun Yat-sen University, Taiwan)

12:42 pm
ID1951: **Low-Complexity and High-Throughput Number Theoretic Transform Architecture for Polynomial Multiplication in Homomorphic Encryption**
Nana Sutisna (Bandung Institute of Technology, IMEC, Indonesia), Elkhan Brillianshah (Bandung Institute of Technology, Indonesia), Infall Syafalni (Bandung Institute of Technology, IMEC,

Indonesia), M. Ogin Hasanuddin (Bandung Institute of Technology, IMEC, Indonesia), Trio Adiono (Bandung Institute of Technology, Indonesia), Tutun Juhana (Bandung Institute of Technology, Indonesia)

11:30 am – 1:00 pm
A2L-04 Hardware Security for IoT, Circuits, & Cyber-Physical Systems I
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Aquarius 4
ORAL
Session Chair(s): Yue Zheng (Chinese University of Hong Kong), Ayesha Khalid (Queen's University of Belfast)

11:30 am
ID2084: CTC: Continuous-Time Convolution Based Multi-Attack Detection for Sensor Networks
Mohammad Monjur (University of New Hampshire, United States), Qiaoyan Yu (University of New Hampshire, United States)

11:48 am
ID2139: A Trusted Inference Mechanism for Edge Computing Based on Post-Quantum Encryption
Yukang Huang (South China University of Technology, China), Junyi Mai (South China University of Technology, China), Wanling Jiang (South China University of Technology, China), Enyi Yao (South China University of Technology, China)

12:06 pm
ID1176: Modular Inversion Architecture Over GF(2^m) Using Optimal Exponentiation Blocks for ECC Cryptosystems
Jingqi Zhang (Beijing Institute of Technology, China), Yujie Jiang (Beijing Institute of Technology, China), An Wang (Beijing Institute of Technology, China)

12:24 pm
ID1680: A Timing Attack Resistant Lightweight Post-Quantum Crypto-Processor for SPHINCS+
Tianze Huang (Huazhong University of Science and Technology, China), Jiahao Lu (Huazhong University of Science and Technology, China), Dongsheng Liu (Huazhong University of Science and Technology, China), Aobo Li (Huazhong University of Science and Technology, China), Shuo Yang (Huazhong University of Science and Technology, China), Lei Chen (Huazhong University of Science and Technology, China), Xiang Li (Huazhong University of Science and Technology, China)

12:42 pm
ID1191: Co-Designing Trusted Execution Environment and Model Encryption for Secure High-Performance DNN Inference on FPGAs
Tsunato Nakai (Mitsubishi Electric Corporation, Japan), Ryo Yamamoto (Mitsubishi Electric Corporation, Japan)

11:30 am – 1:00 pm
A2L-05 Wireline Communications
TRACK 3: COMMUNICATIONS CIRCUITS AND SYSTEMS

Gemini 1
ORAL
Session Chair(s): Zhao Zhang (Institute of Semiconductors, Chinese Academy of Sciences)

11:30 am
ID1235: A Digital Pre-Distortion Technique for High-Linearity, Low-Power, Compact, Phase Interpolators
Zhaowen Wang (Columbia University, United States), Hongzhe Jiang (Columbia University, United States), Peter Kinget (Columbia University, United States)

11:48 am
ID1247: Hadamard Multi-Tone Signaling in Multi-Wire Pulse Amplitude Modulation for Next Generation Wireline Communication
Asif Wahid (University of Utah, United States), Rajath Bindiganavile (University of Utah, United States), Armin Tajalli (University of Utah, United States)

12:06 pm
ID1861: A 4×4 MIMO Discrete Multitone Wireline Transceiver with Far-End Crosstalk Cancellation for ADC-Based High-Speed Serial Links
Jaewon Lee (Daegu Gyeongbuk Institute of Science and Technology, Korea), Seoyoung Jang (Daegu Gyeongbuk Institute of Science and Technology, Korea), Yujin Choi (Daegu Gyeongbuk Institute of Science and Technology, Korea), Donggeun Kim (Daegu Gyeongbuk Institute of Science and Technology, Korea), Matthias Braendli (IBM Research - Zürich, Switzerland), Marcel Kossel (IBM Research - Zürich, Switzerland), Andrea Ruffino (IBM Research - Zürich, Switzerland), Thomas Morf (IBM Research - Zürich, Switzerland), Pier-Andrea Francese (IBM Research - Zürich, Switzerland), Gain Kim (Daegu Gyeongbuk Institute of Science and Technology, Korea)

12:24 pm
ID2217: Minimum Power Point Design of Inverter Based Continuous Time Linear Equalizer (CTLE)
Andrew Ensinger (Oregon State University, United States), Ramin Javadi (Oregon State University, United States), Xiaohui Lin (Oregon State University, United States), Bella Bose (Oregon State University, United States), Tejasvi Anand (Oregon State University, United States)

12:42 pm
ID2420: A 16-Channel Optical Receiver Circuit for a Multicore Fiber-Based Co-Packaged Optics Module in a 65-nm CMOS Chip (TCAS-II paper)
Toshiyuki Inoue (University of Shiga Prefecture, Japan), Akira Tsuchiya (University of Shiga Prefecture, Japan), Keiji Kishine (University of Shiga Prefecture, Japan), Daisuke Ito (Gifu University, Japan), Yasuhiro Takahashi (Gifu University, Japan), Makoto Nakamura (Gifu University, Japan)

11:30 am – 1:00 pm
A2L-06 Integrated Power Circuits & Charge Pumps
TRACK 4: POWER AND ENERGY CIRCUITS AND SYSTEMS

Gemini 2
ORAL
Session Chair(s): Junmin Jiang (Southern University of Science and Technology), Loai Salem (University of California, Santa Barbara)

11:30 am
ID1561: A Fully Integrated LDO Using Synchronous VTC and Asynchronous Step Detection Recovery for Under-1 V Supply Voltage Application
Yufei Sun (Northwestern Polytechnical University, China), Wan Wang (Xi'an Aerosemi Technology, China), Na Kang (Xi'an Aerosemi Technology, China), Jing Fu (Xi'an Aerosemi Technology, China),

Xiaoya Fan (Northwestern Polytechnical University, China), Yanzhao Ma (Northwestern Polytechnical University, China)

11:48 am
ID2225: **A LDO with 5-Na Quiescent Current and Improved Transient Response Within a 50-Ma Load Current Range**
Zaitian Yang (University of Macau, China), Qiujin Chen (University of Macau, China), Shaowei Zhen (University of Electronic Science and Technology of China, China), Mo Huang (University of Macau, China)

12:06 pm
ID1404: **Integrated Cold-Start of a Boost Converter at 54mV Using a Two-Stage Capacitive Voltage Multiplier**
Shaoting Guan (Fudan University, China), Haoyu Jiang (Fudan University, China), Yuxiao Zhao (Fudan University, China), Yifei Huang (Fudan University, China), Hao Min (Fudan University, China)

12:24 pm
ID1740: **A Hybrid High-Voltage Regulating Charge Pump for Electrokinetic Concentration**
Aida Aberra (New York University Abu Dhabi & New York University, U.A.E.), Muhammad Abrar Akram (New York University Abu Dhabi, U.A.E.), Soon-Jae Kweon (Catholic University of Korea, Korea), Jongmin Kim (New York University Abu Dhabi, U.A.E.), Kim-Hoang Nguyen (Korea Advanced Institute of Science and Technology, U.A.E.), Gichan Yun (Korea Advanced Institute of Science and Technology, Kazakhstan), Minkyu Je (Korea Advanced Institute of Science and Technology, Korea), Yong-Ak Song (New York University Abu Dhabi & New York University, Korea), Sohmyng Ha (New York University Abu Dhabi & New York University, U.A.E.)

12:42 pm
ID2136: **A Wide-Bandwidth Supply Modulator Using Binary Switched-Capacitor DC-to-DC Converters**
Loai G. Salem (University of California, Santa Barbara, United States)

11:30 am – 1:00 pm
A2L-07 Neural Interface Circuits & Systems I
TRACK 6: BIOMEDICAL CIRCUITS AND SYSTEMS

Pisces 1
ORAL
Session Chair(s): Yan Liu (Shanghai Jiao Tong University), Julius Georgiou (University of Cyprus)

11:30 am
ID1165: **A 6-μW AC-Coupled, Two-Step Incremental ΔΣ ADC for High-Density Neural Recording**
Xiangwei Zhang (Institute of Microelectronics Chinese Academy of Sciences, China), Wenhao Liu (Institute of Microelectronics Chinese Academy of Sciences, China), Han Yang (Institute of Microelectronics Chinese Academy of Sciences, China), Ying Hou (Institute of Microelectronics Chinese Academy of Sciences, China), Xiaosong Wang (Institute of Microelectronics Chinese Academy of Sciences, China), Yu Liu (Institute of Microelectronics Chinese Academy of Sciences, China)

11:48 am
ID1195: **A Compact Low-Power Bidirectional Two-Wire Interface for Digital Neural Probes**
Daniel De Dorigo (Laboratory for Microelectronics, University of Freiburg, Germany), Roman Willaredt (Laboratory for Microelectronics, University of Freiburg, Germany), Christoph Grandauer (Laboratory for Microelectronics, University of Freiburg, Germany), Daniel Wendler (Laboratory for

Microelectronics, University of Freiburg, Germany), Yiannos Manoli (Laboratory for Microelectronics, University of Freiburg, Germany), Matthias Kuhl (Laboratory for Microelectronics, University of Freiburg, Germany)

12:06 pm
ID1598: A Compressed Sensing Integrate-and-Fire Neuron Concept for Massively Parallel Recordings
Jonas David Rieseler (Hamburg University of Technology, Germany), Christian Adam (Hamburg University of Technology, Germany), Andreas Bahr (Hamburg University of Technology, Germany), Matthias Kuhl (Laboratory for Microelectronics, University of Freiburg, Germany)

12:24 pm
ID1947: A 9.45-ENOB 3.84-MS/s Ping-Pong Interleaving SAR ADC with Integrated Buffers and SPI for 96-Channel Neural Signal Acquisition
Ziqi Li (ShanghaiTech University, China), Xinyue Gu (ShanghaiTech University, China), Hongming Lyu (ShanghaiTech University, China)

12:42 pm
ID2572: NMM-Based Patient-Specific Temporally-Adaptive Stimulation Optimization for Seizure Control
Rojin Salahi (York University, Canada), Hossein Kassiri (York University, Canada)

11:30 am – 1:00 pm
A2L-08 Neural Learning Systems: Optimizations & Applications I
TRACK 8: NEURAL NETWORKS AND NEUROMORPHIC ENGINEERING

Venue: Pisces 2
ORAL
Session Chair(s): Yang Zhao (Shanghai Jiaotong University), Zhongrui Wang (Hongkong University)

11:30 am
ID1562: On Class-Incremental Learning for Fully Binarized Convolutional Neural Network
Yanis Basso-Bert (Université Grenoble Alpes, CEA List, France), William Guicquero (Université Grenoble Alpes, CEA-Leti, France), Anca Molnos (Université Grenoble Alpes, CEA List, France), Romain Lemaire (Université Grenoble Alpes, CEA List, France), Antoine Dupret (Université Grenoble Alpes, CEA-Leti, France)

11:48 am
ID1178: The Initialization Factor: Understanding Its Impact on Active Learning for Analog Circuit Design
Sezin Kircali Ata (Institute for Infocomm Research, Agency for Science, Technology and Research, Singapore), Zhi Hui Kong (Singapore University of Technology and Design, Singapore), Anusha James (Institute for Infocomm Research, Agency for Science, Technology and Research, Singapore), Lile Cai (Institute for Infocomm Research, Agency for Science, Technology and Research, Singapore), Kiat Seng Yeo (Singapore University of Technology and Design, Singapore), Khin Mi Mi Aung (Institute for Infocomm Research, Agency for Science, Technology and Research, Singapore), Chuan Sheng Foo (Institute for Infocomm Research, Agency for Science, Technology and Research, Singapore), Ashish James (Institute for Infocomm Research, Agency for Science, Technology and Research, Singapore)

12:06 pm
ID2484: Model Predictive Control-Based Reinforcement Learning
Qiang Han (University of Western Australia, Australia), Farid Boussaid (University of Western Australia, Australia), Mohammed Bennamoun (University of Western Australia, Australia)

12:24 pm
ID1434: Adaptive Informative Semantic Knowledge Transfer for Knowledge Distillation
Ruijian Xu (Southwest University of Science and Technology, China), Ning Jiang (Southwest University of Science and Technology, China), Jialiang Tang (Nanjing University of Science and Technology, China), Xinlei Huang (Southwest University of Science and Technology, China)

12:42 pm
ID1551: Fast and Lightweight Automatic Modulation Recognition Using Spiking Neural Network
Canghai Lin (National University of Defense Technology, China), Zhijiao Zhang (Independent, China), Lei Wang (Defense Innovation Institute, Academy of Military Sciences, China), Yao Wang (National University of Defense Technology, China), Jingyue Zhao (Defense Innovation Institute, Academy of Military Sciences, China), Zhijie Yang (Defense Innovation Institute, Academy of Military Sciences, China), Xun Xiao (National University of Defense Technology, China)

11:30 am – 1:00 pm
A2L-09 Learning-based Visual Signal Coding & Processing
TRACK 11: VISUAL SIGNAL PROCESSING AND COMMUNICATIONS

Venue: Pisces 3
ORAL
Session Chair(s): Chae Eun Rhee (Inha University), Zhibo Chen (University of Science and Technology of China)

11:30 am
ID1262: Learning-Based Conditional Image Compression
Tianma Shen (Santa Clara University, United States), Wen-Hsiao Peng (National Yang Ming Chiao Tung University, Taiwan), Huang-Chia Shih (Yuan Ze University, Taiwan), Ying Liu (Santa Clara University, United States)

11:48 am
ID1608: Asymmetric Neural Image Compression with High-Preserving Information
Kai Hu (Tianjin University, China), Yu Liu (Tianjin University, China), Fang Xu (Tianjin University & Southwest University, China), Renhe Liu (Tianjin University, China), Han Wang (Tianjin University, China), Shenghui Song (Hong Kong University of Science and Technology, China)

12:06 pm
ID2551: Improved Geometry Coding for Spinning LiDAR Point Cloud Compression
Wenyi Wang (ByteDance Inc., China), Yingzhan Xu (ByteDance Inc., China), Bharath Vishwanath (ByteDance Inc., United States), Kai Zhang (ByteDance Inc., United States), Li Zhang (ByteDance Inc., United States)

12:24 pm
ID1459: SFFTNet: Sparse Feature Fusion Transformer Network for Image Deblurring
Faxing Lei (Fudan University, China), Chao Liu (Fudan University, China), Wei Li (Fudan University, China), Minge Jing (Fudan University, China), Xiankui Xiong (ZTE Corporation, China), Xuanpeng Zhu (ZTE Corporation, China), Yibo Fan (Fudan University, China)

12:42 pm
ID1722: A Resource-Constrained Spatio-Temporal Super Resolution Model
Da Hyeon Jung (Inha University, Korea), Min Wu Jeong (Inha University, Korea), Xuan Truong Nguyen (Seoul National University, Vietnam), Chae Eun Rhee (Inha University, Korea)

11:30 am – 1:00 pm
A2L-10 Cross Society Special Session: Flexible Circuits & Systems for the Era of Everything Intelligence
TRACK 14: SPECIAL SESSION

Venue: Pisces 4
ORAL
Session Chair(s): Xinmiao Zhang (Ohio State University)

11:30 am
ID1998: A 1024-Channel Neurostimulation System Enabled by Photolithographic Organic Thin-Film Transistors with High Uniformity
Bowen Liu (Tsinghua University, China), Yangkun Hou (Tsinghua University, China), Yueshan Qin (Tsinghua University, China), Jiwei Zou (Tsinghua University, China), Hanbin Ma (Suzhou Institute of Biomedical Engineering and Technology of the Chinese Academy of Science, China), Yongpan Liu (Tsinghua University, China), Huazhong Yang (Tsinghua University, China), Xueqing Li (Tsinghua University, China), Chen Jiang (Tsinghua University, China)

11:48 am
ID2150: Squeeze-Excite Fusion Based Multimodal Neural Network for Sleep Stage Classification with Flexible EEG/ECG Signal Acquisition Circuit
Shuailin Tao (Nanyang Technological University, Singapore), Jinhai Hu (Nanyang Technological University, Singapore), Wang Ling Goh (Nanyang Technological University, Singapore), Yuan Gao (Institute of Microelectronics, Agency for Science, Technology and Research, Singapore)

12:06 pm
ID2496: A Large-Area LTPS-TFT-Based Bi-Directional Biomedical Interface with Process-Invariant In-Pixel Biopotential-to-Digital Converters
Hanbo Zhang (Shanghai Jiao Tong University, China), Yuqing Lou (Shanghai Jiao Tong University, China), Zhihang Zhang (Shanghai Jiao Tong University, China), Yongfu Li (Shanghai Jiao Tong University, China), Fakhrul Zaman Rokhani (Universiti Putra Malaysia, Malaysia), Guoxing Wang (Shanghai Jiao Tong University, China), Jian Zhao (Shanghai Jiao Tong University, China)

12:24 pm
ID2500: An Ultra-Low Power Wearable Sensing System with a Highly Sensitive Three-Dimensional LIG Sensor and Energy-Efficient Time Domain Readout
Siyuan Xu (Southern University of Science and Technology, China), Huiru Yang (Southern University of Science and Technology, China), Longhuang Li (Southern University of Science and Technology, China), Yiyang Du (Southern University of Science and Technology, China), Huaiyu Ye (Southern University of Science and Technology, China), Huan Hu (Southern University of Science and Technology, China)

12:42 pm
ID2508: A 2.5 kHz 50.57 dB Linearized VCO ADC Using 6 μm LTPS TFTs
Wangzilu Lu (Shanghai Jiao Tong University, China), Jiajie Huang (Shanghai Jiao Tong University, China), Chao Wang (Shanghai Jiao Tong University, China), Ting Zhou (Shanghai Jiao Tong University, China), Yang Zhao (Shanghai Jiao Tong University, China), Jian Zhao (Shanghai Jiao Tong University, China), Yongfu Li (Shanghai Jiao Tong University, China)

11:30 am – 1:00 pm
A2L-11 Inversion Coefficient & Ratio-based (gm/ID, gm/Cg, etc.) Design Methodologies
TRACK 14: SPECIAL SESSION

Venue: Virgo 1
ORAL
Session Chair(s): Carlos Galup (Universidade Federal de Santa Catarina), Sylvain Bourdel (Grenoble INP - TIMA)

11:30 am
ID1498: A Design-Oriented Single-Piece Short-Channel MOSFET Model
Deni Germano Alves Neto (Federal University of Santa Catarina, Brazil), Gabriel Maranhão (Federal University of Santa Catarina, Brazil), Marcio Cherem Schneider (Federal University of Santa Catarina, Brazil), Carlos Galup-Montoro (Federal University of Santa Catarina, Brazil)

11:48 am
ID1666: A Comprehensive Output Conductance Model Valid in All Regions of Inversion
Christian Enz (École Polytechnique Fédérale de Lausanne, Switzerland), Hung-Chi Han (École Polytechnique Fédérale de Lausanne, Switzerland), Corentin Delignac (Université de Bordeaux, IMS Laboratory, France), Thierry Taris (Université de Bordeaux, IMS Laboratory, France)

12:06 pm
ID1668: Practical Aspects of Script-Based Analog Design Using Precomputed Lookup Tables
Boris Murmann (University of Hawaii, United States)

12:24 pm
ID2152: A gm/Id Based Methodology to Estimate OTA Requirements in Low-Pass Discrete Time ΣΔ-ADCs
Ali Mostafa (Université Grenoble Alpes, CEA-Leti, France), João Roberto Raposo Martins (2X-FAB Semiconductor Foundries, France), Jérôme Juillard (Université Paris-Saclay, CentraleSupélec, CNRS, GeePs, Sorbonne Université, France), Pietro Maris Ferreira (Université Paris-Saclay, CentraleSupélec, CNRS, GeePs, Sorbonne Université, France)

12:42 pm
ID2248: Dynamic Analysis of RF CMOS Inverter-Based Ring Oscillators Using an All-Region MOSFET Charge-Based Model in 28nm FD-SOI CMOS
Julien Poupon (STMicroelectronics, France), Manuel Barragan (Laboratoire TIMA; Université Grenoble Alpes, France), Andreia Cathelin (STMicroelectronics, France), Sylvain Bourdel (Laboratoire TIMA; Grenoble Institute of Technology, France)

11:30 am – 1:00 pm
A2L-12 Novel Hardware Implementation of Learning Algorithms in Deep & Spiking Neural Networks I
TRACK 14: SPECIAL SESSION

Venue: Virgo 2
ORAL
Session Chair(s): Amirali Amirsoleimani (Lassonde School of Engineering at York University), Mostafa Rahimi Azghadi (James Cook University)

11:30 am
ID1665: Efficient Reinforcement Learning on Passive RRAM Crossbar Array
Arjun Tyagi (University of Illinois Urbana-Champaign, United States), Shubham Sahay (Indian Institute of Technology Kanpur, India)

11:48 am
ID1769: **An FPGA Implementation of an Event-Driven Unsupervised Feature Extraction Algorithm for Pattern Recognition**
Philip Chennakudy Jose (International Centre for Neuromorphic Systems, Australia), Ying Xu (International Centre for Neuromorphic Systems, Australia), André van Schaik (Western Sydney University, Australia), Runchun Wang (International Centre for Neuromorphic Systems, Australia)

12:06 pm
ID1774: **BitPruning: Learning Bitlengths for Aggressive and Accurate Quantization**
Miloš Nikolić (University of Toronto, Canada), Ghouthi Boukli Hacene (Mila - Quebec AI Institute, Canada), Ciaran Bannon (University of Toronto, Canada), Alberto Delmas Lascorz (University of Toronto, Canada), Matthieu Courbariaux (Mila - Quebec AI Institute, Canada), Omar Mohamed Awad (University of Toronto, Canada), Isak Edo Vivancos (University of Toronto, Canada), Yoshua Bengio (Mila - Quebec AI Institute, Canada), Vincent Gripon (IMT Atlantique Bretagne-Pays de la Loire, Lab-STICC, France), Andreas Moshovos (University of Toronto, Canada)

12:24 pm
ID2070: **Equilibrium-Based Learning Dynamics in Spiking Architectures**
Malyaban Bal (Pennsylvania State University, United States), Abhronil Sengupta (Pennsylvania State University, United States)

12:42 pm
ID2154: **Advancing Image Classification with Phase-Coded Ultra-Efficient Spiking Neural Networks**
Zhengyu Cai (University of Toronto, Canada), Hamid Rahimian Kalatehbali (York University, Canada), Ben Walters (James Cook University, Australia), Mostafa Rahimi Azghadi (James Cook University, Australia), Roman Genov (University of Toronto, Canada), Amirali Amirsoleimani (York University, Canada)

11:30 am – 1:00 pm
A2L-13 RFIC & AI: Pioneering New Wireless Communications
TRACK 14: SPECIAL SESSION

Venue: Virgo 3
ORAL
Session Chair(s): Francois Rivet (University of Bordeaux)

11:30 am
ID1826: **OpenDPD: An Open-Source End-to-End Learning & Benchmarking Framework for Wideband Power Amplifier Modeling and Digital Pre-Distortion**
Yizhuo Wu (Delft University of Technology, Netherlands), Gagan Deep Singh (Delft University of Technology, Netherlands), Mohammad Reza Beikmirza (Delft University of Technology, Netherlands), Leo C. N. de Vreede (Delft University of Technology, Netherlands), Morteza Alavi (Delft University of Technology, Netherlands), Chang Gao (Delft University of Technology, Netherlands)

11:48 am
ID1554: **Co-Simulation Workflow for D-Band Power Amplifier Linearization Using Walsh-Based DPD**
Antoine Lhomel (Université de Bordeaux, IMS Laboratory, France), Maxandre Fellmann (Université de Bordeaux, IMS Laboratory, France), Yann Deval (Université de Bordeaux, IMS Laboratory, France), Eric Kerhervé (Université de Bordeaux, IMS Laboratory, France), François Rivet (Université de Bordeaux, IMS Laboratory, France), Nathalie Deltimple (Université de Bordeaux, IMS Laboratory, France)

12:06 pm
ID2029: [Walsh-Domain Neural Network for Power Amplifier Behavioral Modelling and Digital Predistortion]
Cel Thys (Katholieke Universiteit Leuven, Belgium), Rodney Martinez Alonso (Katholieke Universiteit Leuven, Belgium), Antoine Lhomel (Université de Bordeaux, IMS Laboratory, France), Maxandre Fellmann (Université de Bordeaux, IMS Laboratory, France), Nathalie Deltimple (Université de Bordeaux, IMS Laboratory, France), François Rivet (Université de Bordeaux, IMS Laboratory, France), Sofie Pollin (Katholieke Universiteit Leuven, Belgium)

12:24 pm
ID1199: [Artificial-Intelligence-Driven RF Carrier Aggregation Filter for 6G Application]
Pierre Courouve (Université Grenoble Alpes, CEA-Leti, France), Ali Al Shakoush (Université Grenoble Alpes, CEA-Leti, France), Cedric Dehos (Université Grenoble Alpes, CEA-Leti, France), Laurent Ouvry (Université Grenoble Alpes, CEA-Leti, France)

1:00 pm – 2:00 pm
Lunch
NETWORKING

Venue: B2 Ballroom

2:00 pm – 3:00 pm
Keynote: More Sustainable Bio/CMOS Interfaces for Remote Human Health
KEYNOTE

Venue: B2 Ballroom
Speaker: Sandro Carrara, Professor, Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland
Session Chair(s): Victor Grimblatt (Synopsys)

3:00 pm – 6:30 pm
Climate Change
EMBEDDED WORKSHOP

Venue: Leo 1
Session Chair(s): Dr Balwant Godara (Political advisor at SWA, the UN-hosted partnership on water USA/Switzerland)

3:00 pm – 4:30 pm
CASS Mentoring
SPECIAL EVENT

Venue: Virgo 4
Session Chair(s): Yu Wu (University College London, UK)

3:00 pm – 4:30 pm
A3L-01 LDO Regulators
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Aquarius 1
ORAL

Session Chair(s): Filippo Neri (Renesas Electronics, Zürich, Switzerland), Yanhan Zeng (Guangzhou University)

3:00 pm
ID2398: A Capacitor-Less LDO Regulator Compensated by Adaptive Zero for Zero-Load Stability Enhancement
Shengping Lv (Tsinghua University & Beijing University of Technology, China), Zhijie Chen (Beijing University of Technology, China), Peng Zhang (HexinHulian Technology (Beijing) Co., Ltd., China), Peiyuan Wan (Beijing University of Technology, China), Liuxin Lv (Tsinghua University, China), Hanjun Jiang (Tsinghua University, China)

3:18 pm
ID1364: A Fast Transient PMOS LDO with AP3 Buffer and Shaped-Hybrid-Bias EA Techniques Achieving 8.15ps FOM
Xin-Ce Gong (University of Electronic Science and Technology of China, China), Jian-Jun Kuang (University of Electronic Science and Technology of China, China), Xin Ming (University of Electronic Science and Technology of China, China), Zhi-Yi Lin (University of Electronic Science and Technology of China, China), Bo Zhang (University of Electronic Science and Technology of China, China)

3:36 pm
ID1944: A Fast Transient Response Capless LDO Regulator Achieving -78 dB of PSR Up to 2 MHz
Xiang Cheng (University of Electronic Science and Technology of China, China), Huihua Liu (University of Electronic Science and Technology of China, China), Jingzhi Zhang (University of Electronic Science and Technology of China, China), Yiming Yu (University of Electronic Science and Technology of China, China), Yunqiu Wu (University of Electronic Science and Technology of China, China), Chenxi Zhao (University of Electronic Science and Technology of China, China), Kai Kang (University of Electronic Science and Technology of China, China)

3:54 pm
ID2546: A Tri-Loop Capacitor-Less LDO with Current Feedback Loop and Super Source Follower Achieving 8-mV Undershoot and 99-dB PSR
Jiahao Liu (Southeast University, China), Wangchen Fan (Southeast University, China), Yiqing Wang (Southeast University, China), Weifeng Sun (Southeast University, China), Zhongyuan Fang (Southeast University, China)

4:12 pm
ID1588: A Capacitor-Less Hybrid LDO for Low Frequency Supply Noise Suppression Achieving 99.87% Efficiency and 3.32ps Response Time in 65nm
Yaswanth Kumar Cherivirala (University of Michigan, United States), David Wentzloff (University of Michigan, United States)

3:00 pm – 4:30 pm
A3L-02 AI & ML techniques for Non-Linear Circuits & Systems
TRACK 9: METHODS AND MODELS FOR THE ANALYSIS/DESIGN OF NONLINEAR CIRCUITS AND SYSTEMS

Aquarius 2
ORAL
Session Chair(s): Erivelton Nepomuceno (Maynooth University- Ireland), Mohammed Fouda (University of California, USA)

3:00 pm
ID1752: Spectral Structure Analysis of FFT-Based Digital Predistortion for Wideband 5G Applications
Tayeb Habib Chawki Bouazza (Telecom Paris, France), Dang-Kièn Germain Pham (Telecom Paris, France), Reda Mohellebi (Telecom Paris, France), Patricia Desgreys (Telecom Paris, France)

3:18 pm
ID2383: Enhancing ML Model Accuracy for Digital VLSI Circuits Using Diffusion Models: A Study on Synthetic Data Generation
Prasha Srivastava (International Institute of Information Technology Hyderabad, India), Pawan Kumar (International Institute of Information Technology Hyderabad, India), Zia Abbas (International Institute of Information Technology Hyderabad, India)

3:36 pm
ID1457: Predicting Higher-Order Dynamics Without Network Topology by Ridge Regression
Zili Zhou (Fudan University, China), Cong Li (Fudan University, China), Bo Qu (Guangdong University of Science and Technology, China), Xiang Li (Tongji University, China)

3:54 pm
ID1886: LQR and Genetic Algorithms: An Effective Duo for Assessing Control Expenditure and Performance in Dynamic Systems
Josefredo Gadelha da Silva (Maynooth University, Ireland), Marcio Lacerda (Federal University of Sao Joao del Rei, Brazil), Ariadne Bertolin (Maynooth University, Ireland), Jander Santos (Federal University of Sao Joao del Rei, Brazil), Erivelton Nepomuceno (Maynooth University, Ireland)

4:12 pm
ID1932: ESFLOW: Mapping Large-Scale Earthquake Simulation to Spatial Computing Systems
Ming Yuan (Tianjin University, China), Qiang Liu (Tianjin University, China), Lin Gan (Tsinghua University, China), Guangwen Yang (Tsinghua University, China)

3:00 pm – 4:30 pm
A3L-03 Low Power Logic, Circuits & Architectures I
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Aquarius 3
ORAL
Session Chair(s): Ettore Napoli (Università degli Studi di Salerno), Naeem Abbasi (Qualcomm)

3:00 pm
ID2377: An Ultra Low Voltage Energy Efficient Level Shifter with Current Limiter and Improved Split-Controlled Inverter (TCAS-II paper)
Chao Wang (Shanghai Jiao Tong University, China), Yang Wei Lim (Universiti Putra Malaysia, Malaysia), Yuxin Ji (Shanghai Jiao Tong University, China), Jiajie Huang (Shanghai Jiao Tong University, China), Wangzilu Lu (Shanghai Jiao Tong University, China), Fakhrul Zaman Rokhani (Universiti Putra Malaysia, Malaysia), Yehea Ismail (American University in Cairo, Egypt), Yongfu Li (Shanghai Jiao Tong University, China),

3:18 pm
ID2129: A Redundant-Transition-Free and Contention-Free Change-Sensing Flip-Flop (TCAS-II paper)
Kyounghun Kang (Korea Advanced Institute of Science and Technology, Korea), Wanyeong Jung (Korea Advanced Institute of Science and Technology, Korea)

3:36 pm
ID1846: Hardware Accelerator for Feature Matching with Binary Search Tree
Aruma Hannadige Miyuru Thathsara (Nanyang Technological University, Singapore), Siew-Kei Lam (Nanyang Technological University, Singapore), Damith Anhettigama Kawshan (Nanyang Technological University, Singapore), Duvindu Piyasena (Nanyang Technological University, Singapore)

3:54 pm
ID2036: A 3.2-GHz 0.3/0.5 V 16-nm FinFET I/O Buffer with Low-Power PVT Compensation Circuit
Tzung-Je Lee (National Sun Yat-sen University, Taiwan), Ji-Hau Chiou (National Sun Yat-sen University, Taiwan)

4:12 pm
ID2535: A Hyperdimensional Computing Architecture with 4.4x Energy Efficiency in 65nm CMOS
Fredrick Angelo Galapon (University of the Philippines Diliman, Philippines), Anastacia Alvarez (University of the Philippines Diliman, Philippines)

3:00 pm – 4:30 pm
A3L-04 Digital Circuits, Systems & Architecture for Machine Learning I
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Aquarius 4
ORAL
Session Chair(s): Bo Wang (SUTD), Preet Yadav (NXP Semiconductors, India)

3:00 pm
ID1087: SuperHCA: A Super-Resolution Accelerator with Sparsity-Aware Heterogeneous Core Architecture
Zhicheng Hu (University of Electronic Science and Technology of China, China), Jiahao Zeng (University of Electronic Science and Technology of China, China), Xin Zhao (University of Electronic Science and Technology of China, China), Liang Zhou (University of Electronic Science and Technology of China, China), Liang Chang (University of Electronic Science and Technology of China, China)

3:18 pm
ID1447: A Precision-Scalable Vision Accelerator for Robotic Applications
Haoran Zeng (Nanjing University, China), Wendong Mao (Sun Yat-sen University, China), Siyu Zhang (Nanjing University, China), Zhongfeng Wang (Nanjing University, China)

3:36 pm
ID2241: An Edge AI Accelerator Design Based on HDC Model for Real-Time EEG-Based Emotion Recognition System with RISC-V FPGA Platform
Jia-Yu Li (National Yang Ming Chiao Tung University, Institute of Electronics, Taiwan), Wai-Chi Fang (National Yang Ming Chiao Tung University, Taiwan)

3:54 pm
ID1791: Efficient FPGA Resource Utilization in Wired-Logic Processors Using Coarse and Fine Segmentation of LUTs for Non-Linear Functions
Dongzhu Li (University of Tokyo, Japan), Tianqi Zhao (Tsinghua University, China), Kenji Kobayashi (University of Tokyo, Japan), Atsutake Kosuge (University of Tokyo, Japan), Mototsugu Hamada (University of Tokyo, Japan), Tadahiro Kuroda (University of Tokyo, Japan)

4:12 pm
ID1062: High-Utilization GPGPU Design for Accelerating GEMM Workloads: An Incremental Approach
Chongxi Wang (University of the Chinese Academy of Sciences, China), Penghao Song (University of the Chinese Academy of Sciences, China), Haoyu Zhao (State Key Lab of Processors, Institute of Computing Technology, Chinese Academy of Sciences, China), Fuxin Zhang (State Key Lab of Processors, Institute of Computing Technology, Chinese Academy of Sciences, China), Jian Wang (State Key Lab of Processors, Institute of Computing Technology, Chinese Academy of Sciences, China), Longbing Zhang (State Key Lab of Processors, Institute of Computing Technology, Chinese Academy of Sciences, China)

3:00 pm – 4:30 pm
A3L-05 Optical Communications
TRACK 3: COMMUNICATIONS CIRCUITS AND SYSTEMS

Venue: Gemini 1
ORAL
Session Chair(s): Jongsun Park (Korea University)

3:00 pm
ID1122: FPGA Implementation of SFO for OFDM-Based Network Enabled Li-Fi System
Trio Adiono (Bandung Institute of Technology, Indonesia), Erwin Setiawan (Bandung Institute of Technology, Indonesia), Michael Jonathan (Bandung Institute of Technology, Indonesia), Rahmat Mulyawan (Bandung Institute of Technology, Indonesia), Nana Sutisna (Bandung Institute of Technology, IMEC, Indonesia), Infall Syafalni (Bandung Institute of Technology, IMEC, Indonesia), Wasiu Popoola (University of Edinburgh, United Kingdom)

3:18 pm
ID1689: 3D-Integrated, Low Power, High Bandwidth Density Opto-Electronic Transceiver
Devesh Khilwani (Cornell University, United States), Sunwoo Lee (Nanyang Technological University, Singapore), Christine Ou (Cornell University, United States), Stuart Daudlin (Columbia University, United States), Anthony Rizzo (Columbia University, United States), Songli Wang (Columbia University, United States), Michael Cullen (Columbia University, United States), Keren Bergman (Columbia University, United States), Alyosha Molnar (Cornell University, United States)

3:36 pm
ID1749: A 32Gb/s NRZ Low-Bias DFB Driver with Frequency Boosting for High Efficiency Data Transmission
Yang Min (Institute of Microelectronics Chinese Academy of Sciences, University of Chinese Academy of Sciences, China), Yi Zhang (Institute of Semiconductors, Chinese Academy of Sciences, China), Tao Yang (Institute of Semiconductors, Chinese Academy of Sciences, China), Leliang Li (Institute of Semiconductors, Chinese Academy of Sciences, China), Guike Li (Institute of Semiconductors, Chinese Academy of Sciences, China), Zhao Zhang (Institute of Microelectronics Chinese Academy of Sciences, University of Chinese Academy of Sciences, China), Jian Liu (Institute of Microelectronics Chinese Academy of Sciences, University of Chinese Academy of Sciences, China), Nanjian Wu (Institute of Microelectronics Chinese Academy of Sciences, University of Chinese Academy of Sciences, China), Yonghui Lin (UX High-speed IC Co.,LTD., China), Huiyao Peng (UX High-speed IC Co.,LTD, China), Jingbo Shi (Beijing University of Posts and Telecommunications, China), Nan Qi (Institute of Microelectronics Chinese Academy of Sciences, University of Chinese Academy of Sciences, China)

3:54 pm
ID1844: A Sub-1pJ/Bit Laser Power Independent 32Gb/s Silicon Photonic EAM Driver in 65nm CMOS

Shubham Mishra (University of Delaware, United States), Vishal Saxena (University of Delaware, United States)

4:12 pm
ID2338: Linearity Enhancement Analysis of Breakdown Voltage Doubler and Demonstration in 60 GBd SiGe BiCMOS Driver
Kieran De Bruyn (Ghent University - imec, Belgium), Tinus Pannier (Ghent University - imec, Belgium), Jakob Declercq (Ghent University - imec, Belgium), Laurens Breyne (Ghent University - imec, Nokia Bell Labs, Belgium), Xin Yin (Ghent University - imec, Belgium), Peter Ossieur (Ghent University - imec, Belgium), Johan Bauwelinck (Ghent University - imec, Belgium)

3:00 pm – 4:30 pm
A3L-06 Circuits & Systems for Energy Harvesting
TRACK 4: POWER AND ENERGY CIRCUITS AND SYSTEMS

Venue: Gemini 2
ORAL
Session Chair(s): Sijun Du (Delft University of Technology), Zhiyuan Chen (Fudan University)

3:00 pm
ID1081: A 409mV, Sub-10nW Power-on Reset Circuit Using Adaptive Accuracy Adjustment for Low Voltage Applications
Heng You (Nanjing Institute of Intelligent Technology, China), Dashan Shi (Shanghai Electro-Mechanical Engineering Institute, China), Delong Shang (Nanjing Institute of Intelligent Technology, China), Yumei Zhou (Institute of Microelectronics Chinese Academy of Sciences, University of Chinese Academy of Sciences, China), Shushan Qiao (Institute of Microelectronics Chinese Academy of Sciences, China)

3:18 pm
ID2231: An 884MHz, −41.8dBm Input Power Sensitivity, 570-Stage CMOS RF-DC Rectifier with Ground Shielded Input Coupling Capacitors
Yoomi Park (Dongguk University, Korea), Sangjin Byun (Dongguk University, Korea)

3:36 pm
ID1905: A Synchronous Current Inversion and Energy Extraction Circuit for Electromagnetic Energy Harvesting
Jiacong Qiu (ShanghaiTech University, China), Junrui Liang (ShanghaiTech University, China)

3:54 pm
ID2320: An Efficient Rectifier Hybridizing Synchronized Electric Charge Extraction and Bias-Flipping for Triboelectric Energy Harvesting
Wenyu Peng (Delft University of Technology, Netherlands), Willem van Driel (Delft University of Technology, Netherlands), Guoqi Zhang (Delft University of Technology, Netherlands), Sijun Du (Delft University of Technology, Netherlands)

3:00 pm – 4:30 pm
A3L-07 Neural Interface Circuits & Systems II
TRACK 6: BIOMEDICAL CIRCUITS AND SYSTEMS

Pisces 1
ORAL
Session Chair(s): Hanjun Jiang (Tsinghua University, China), Donald Lie (Texas Tech University)

3:00 pm
ID2176: An Area-Efficient, DC-Coupled VCO-Based CT ΔΣM with Input-TR-DAC for Neural Recording
Woobean Lee (Korea Advanced Institute of Science and Technology, Korea), Yoontae Jung (Korea Advanced Institute of Science and Technology, Korea), Hyuntak Jeon (Chungbuk National University, Korea), Jimin Koo (Korea Advanced Institute of Science and Technology, Korea), Sein Oh (Korea Advanced Institute of Science and Technology, Korea), Soon-Jae Kweon (Catholic University of Korea, Korea), Minkyu Je (Korea Advanced Institute of Science and Technology, Korea)

3:18 pm
ID2280: A Microwatt/Channel Neural Signal Processor for High-Channel-Count Spike Detection and Sorting
Zichen Hu (ShanghaiTech University, China), Zhining Zhou (ShanghaiTech University, China), Hongming Lyu (ShanghaiTech University, China)

3:36 pm
ID1148: A Stimulation Artifacts Removal Technique Employing VCO and Phase Detector for Simultaneous Neural Stimulation and Recording
Wenjie Wang (Southeast University, China), Jianan Zheng (Southeast University, China), Yang Zhou (Southeast University, China), Risheng Su (Southeast University, China), Longbin Zhu (Southeast University, China), Zhijun Zhou (Southeast University, China)

3:54 pm
ID1486: A 0.04 mm²/Channel Neural Amplifier with an Input-Referred Noise of 4.6 μVrms and Power Consumption of 3 μW
Huiyong Zheng (Fudan University, China), Yukun Ding (Fudan University, China), Xiao Liu (Fudan University, China)

4:12 pm
ID2300: A μW-Level Multi-Channel Calibration-Free Spike Detector with High Accuracy Based on Stationary Wavelet Transform and Teager Energy Operators
Zhining Zhou (ShanghaiTech University, China), Zichen Hu (ShanghaiTech University, China), Hongming Lyu (ShanghaiTech University, China)

3:00 pm – 4:30 pm
A3L-08 Neural Learning Systems: Transformers & Applications I
TRACK 8: NEURAL NETWORKS AND NEUROMORPHIC ENGINEERING

Pisces 2
ORAL
Session Chair(s): Chang Gao (TU Delft), Huanglong Li (Tsinghua University)

3:00 pm
ID1527: Retraining-Free Constraint-Aware Token Pruning for Vision Transformer on Edge Devices
Yun-Chia Yu (National Taiwan University, Taiwan), Mao-Chi Weng (National Taiwan University, Taiwan), Ming-Guang Lin (National Taiwan University, Taiwan), An-Yeu Wu (National Taiwan University, Taiwan)

3:18 pm
ID1617: Similarity-Aware Fast Low-Rank Decomposition Framework for Vision Transformers

Yuan-June Luo (National Taiwan University, Taiwan), Yu-Shan Tai (National Taiwan University, Taiwan), Ming-Guang Lin (National Taiwan University, Taiwan), An-Yeu Wu (National Taiwan University, Taiwan)

3:36 pm
ID1139: Human Activity Recognition Using Wi-Fi Signals Based on Tokenized Signals with Attention
Jaekwon Lee (Yonsei University, Korea), Lu Zhang (Yonsei University, Korea), Donghyun Kim (Yonsei University, Korea), Kar-Ann Toh (Yonsei University, Korea)

3:54 pm
ID1713: Domain Generalization with Anti-Background Perturbation Consistency and Texture Reduction Ensemble Models for Hepatocyte Nucleus Segmentation
Yu-Ting Wu (National Cheng Kung University, Taiwan), Hung-Wen Tsai (National Cheng Kung University Hospital, Taiwan), Pau-Choo Chung (National Cheng Kung University, Taiwan), Chein-I Chang (National Cheng Kung University, Taiwan), Nien-Tsu Li (National Cheng Kung University, Taiwan), Yu-Xian Huang (National Cheng Kung University, Taiwan), Kuo-Sheng Cheng (National Cheng Kung University, Taiwan)

4:12 pm
ID1754: Epilepsy Seizure Detection and Prediction Using an Approximate Spiking Convolutional Transformer
Qinyu Chen (University of Zürich & ETH Zürich, Switzerland), Congyi Sun (Nanjing University, China), Chang Gao (Delft University of Technology, Netherlands), Shih-Chii Liu (University of Zürich & ETH Zürich, Switzerland)

3:00 pm – 4:30 pm
A3L-09 Image/Video Coding & Standardization
TRACK 11: VISUAL SIGNAL PROCESSING AND COMMUNICATIONS

Venue: Pisces 3
ORAL
Session Chair(s): Yibo Fan (Fudan University), Xin Jin (Tsinghua University)

3:00 pm
ID1506: CTU-Level Adaptive Quantization Method Joint with GOP Based Temporal Filter for Video Coding
Chenlong He (Fudan University, China), Wei Li (Fudan University, China), Xiaoxiang Chen (Fudan University, China), Zhijian Hao (Fudan University, China), Chao Liu (Fudan University, China), Xiaoyang Zeng (Fudan University, China), Yibo Fan (Fudan University, China)

3:18 pm
ID1539: An 8K@120fps Hardware Implementation for Decoder-Side Motion Vector Refinement in VVC
Jiahao Liu (Fudan University, China), Leilei Huang (East China Normal University, China), Shushi Chen (Fudan University, China), Wei Li (Fudan University, China), Yibo Fan (Fudan University, China)

3:36 pm
ID1543: Region Motion-Based Adaptive Composite Long-Term Reference Coding for VVC
Xiaozhen Zheng (Tsinghua Shenzhen International Graduate School, China), Yu Liu (University of Electronic Science and Technology of China, China), Jianglin Wang (SZ DJI Technology Co., Ltd, China), Zihao Ren (University of Electronic Science and Technology of China, China), Shuyuan Zhu

(University of Electronic Science and Technology of China, China), Qingmin Liao (Tsinghua University, China)

3:54 pm
ID2426: Self-Aware Cross-Component Prediction Model Based on Template for Screen Content Coding
Kun Zhang (Sun Yat-sen University, China), Hongxin Qiu (Sun Yat-sen University, China), Zhikai Liu (Sun Yat-sen University, China), Fan Liang (Sun Yat-sen University, China), Wei Sun (Sun Yat-sen University, China)

3:00 pm – 4:30 pm
A3L-10 Optical & Wireless Communication & Sensing Technologies in Terrestrial & Non-Terrestrial Systems for 6G I
TRACK 14: SPECIAL SESSION

Pisces 4
ORAL
Session Chair(s): Shintaro Arai (Okayama University of Science), Di He (Shanghai Jiao Tong University)

3:00 pm
ID1188: Experimental Demonstration of Dual Camera Receivers in M-PAM Rolling Shutter Based Visible Light Communication
Azuki Takada (Chiba Institute of Technology, Japan), Masayuki Kinoshita (Chiba Institute of Technology, Japan), Koji Kamakura (Chiba Institute of Technology, Japan), Takaya Yamazato (Nagoya University, Japan)

3:18 pm
ID1807: CLFusion:3D Semantic Segmentation Based on Camera and LiDAR Fusion
Tianyue Wang (University of Electronic Science and Technology of China, China), Rujun Song (University of Electronic Science and Technology of China, China), Zhuoling Xiao (University of Electronic Science and Technology of China, China), Bo Yan (University of Electronic Science and Technology of China, China), Haojie Qin (University of Electronic Science and Technology of China, China), Di He (Shanghai Jiao Tong University, China)

3:36 pm
ID1532: Performance Analysis of Underwater Optical Wireless Video Communication Systems
Rajeev Kumar Kottilingal (Indian Institute of Technology Goa, India), Nandakumar Nambath (Indian Institute of Technology Goa, India)

3:54 pm
ID1604: Handover Management Through Reconfigurable Intelligent Surfaces for VLC Under Blockage Conditions
Kapila W. S. Palitharathna (University of Cyprus, Cyprus), Anna Maria Vegni (Roma Tre University, Italy), Panagiotis D. Diamantoulakis (University of Macedonia, Greece), Himal A. Suraweera (University of Peradeniya, Sri Lanka), Ioannis Krikidis (University of Cyprus, Cyprus)

4:12 pm
ID2589: Selective Diversity Reception in Underwater Optical Camera Communication
Yuta Furukawa (Tokyo University of Science, Japan), Yuki Sasaki (Tokyo University of Science, Japan), Daisuke Hisano (Osaka University, Japan), Yu Nakayama (Tokyo University of Agriculture and Technology, Japan), Kazuki Maruta (Tokyo University of Science, Japan)

3:00 pm – 4:30 pm
A3L-11 Innovations in Computational Intelligence: Studies on Structures, Detection, & Optimization
TRACK 14: SPECIAL SESSION

Virgo 1
ORAL
Session Chair(s): Haruna Matsushita (Kagawa University), Kenya Jin'no (Tokyo City University)

3:00 pm
ID1693: A Study on Hybrid Optimization Methods Using Lévy Flight and Differential Evolution Mechanisms
Takuya Shindo (Nippon Institute of Technology, Japan), Nobhiko Itoh (Nippon Institute of Technology, Japan)

3:18 pm
ID2109: Analysis for Optimizer Based on Spiking-Neural Oscillator Networks with a Simple Network Topology
Tomoyuki Sasaki (Shonan Institute of Technology, Japan), Hidehiro Nakano (Tokyo City University, Japan)

3:36 pm
ID2191: Derivative-Free-Optimization-Based Bifurcation Point Detection Method Without Parameter Tuning
Haruna Matsushita (Kagawa University, Japan), Hiroaki Kurokawa (Tokyo University of Technology, Japan), Takuji Kousaka (Chukyo University, Japan)

3:54 pm
ID2232: Detection of Fake Images Focused on Few Local Blocks
Takumi Owada (Tokyo City University, Japan), Kenya Jin'no (Tokyo City University, Japan)

4:12 pm
ID2367: A Routing Method Using Chaotic Neurodynamics for the Transportation Networks with the Next Generation Vehicles
Takatoshi Inaba (Nippon Institute of Technology, Japan), Konosuke Hiraki (Nippon Institute of Technology, Japan), Takafumi Matsuura (Nippon Institute of Technology, Japan), Takayuki Kimura (Nippon Institute of Technology, Japan)

3:00 pm – 4:30 pm
A3L-12 Novel Hardware Implementation of Learning Algorithms in Deep & Spiking Neural Networks II
TRACK 14: SPECIAL SESSION

Virgo 2
ORAL
Session Chair(s): Amirali Amirsoleimani (Lassonde School of Engineering at York University), Mostafa Rahimi Azghadi (James Cook University)

3:00 pm
ID2471: Spiking-HDC: A Spiking Neural Network Processor with HDC Classifier Enabling Transfer Learning
Anqin Xiao (Fudan University, China), Xin Zhang (Fudan University, China), Jinqiao Yang (Fudan University, China), Lirong Zheng (Fudan University, China), Zhuo Zou (Fudan University, China)

3:18 pm
ID1402: **A Multi-Stride Convolution Acceleration Algorithm for CNNs**
Anaam Ansari (Santa Clara University, United States), Tokunbo Ogunfunmi (Santa Clara University, United States)

3:36 pm
ID1456: **A Physical Reservoir Computing Processor for ECG-to-PCG Signals Prediction**
Yuqi Ding (University of Glasgow, United Kingdom), Haobo Li (University of Glasgow, United Kingdom), Xiangpeng Liang (Tsinghua University, China), Marija Vaskeviciute (University of Glasgow, United Kingdom), Daniele Faccio (University of Glasgow, United Kingdom), Hadi Heidari (University of Glasgow, United Kingdom)

3:54 pm
ID2022: **Securing On-Chip Learning: Navigating Vulnerabilities and Potential Safeguards in Spiking Neural Network Architectures**
Najmeh Nazari (University of California, Davis, United States), Kevin Immanuel Gubbi (University of California, Davis, United States), Banafsheh Saber Latibari (University of California, Davis, United States), Muhtasim Chowdhury (University of Arizona, United States), Chongzhou Fang (University of California, Davis, United States), Avesta Sasan (University of California, Davis, United States), Setareh Rafatirad (University of California, Davis, United States), Houman Homayoun (University of California, Davis, United States), Soheil Salehi (University of Arizona, United States)

3:00 pm – 4:30 pm
A3L-13 Delta-Sigma ADCs & its AI application
TRACK 14: SPECIAL SESSION

Virgo 3
ORAL
Session Chair(s): Qiang Li (University of Electronic Science and Technol), Liang Qi (Shanghai Jiao Tong University)

3:00 pm
ID2413: **A Delta-Sigma-Based Computing-in-Memory Macro Targeting Edge Computation**
Ran Zhang (University of Macau, Macau), Ka-Fai Un (University of Macau, Macau), Mingqiang Guo (University of Macau, Macau), Liang Qi (Shanghai Jiao Tong University, China), Dengke Xu (Amicro Semiconductor Company Ltd., China), Weibing Zhao (Amicro Semiconductor Company Ltd., China), Rui Paulo Da Silva Martins (University of Macau, Macau), Franco Maloberti (University of Pavia, Italy), Sai-Weng Sin (University of Macau, Macau)

3:18 pm
ID1784: **DAC Element Mismatch Shaping Algorithms in Incremental Delta-Sigma ADCs**
Omar Ismail (Universität Ulm, Germany), Paul Kaesser (Universität Ulm, Germany), John Kauffman (Universität Ulm, Germany), Maurits Ortmanns (Universität Ulm, Germany)

3:36 pm
ID1759: **Stability Prediction of ΔΣ Modulators Using Artificial Neural Networks**
Paul Kaesser (Universität Ulm, Germany), Sebastian Kaltenstadler (Universität Ulm, Germany), Joschua Conrad (Universität Ulm, Germany), Johannes Wagner (Universität Ulm, Germany), Omar Ismail (Universität Ulm, Egypt), Maurits Ortmanns (Universität Ulm, Germany)

3:54 pm
ID2486: **A 0.5V 723nW 84.3dB-SNDR Dynamic Zoom ADC with CLS-Assisted Capacitively-Biased FIA**

Weiqiang Chen (Zhejiang University, China), Lingxin Meng (Zhejiang University, China), Yining Zhao (Zhejiang University, China), Menglian Zhao (Zhejiang University, China), Zhichao Tan (Zhejiang University, China)

4:12 pm
ID2493: Comparative Study for Different Loop-Filter Architectures of 2x Time-Interleaved CT DSM
Meng Guo (Shanghai Jiao Tong University, China), Yuekai Liu (Shanghai Jiao Tong University, China), Jinlei Pan (Shanghai Jiao Tong University, China), Liang Qi (Shanghai Jiao Tong University, China)

3:00 pm – 3:30 pm
Coffee Break
NETWORKING

4:30 pm – 6:30 pm
PhD Forum (Poster)
SPECIAL EVENT

Venue: Leo 2+3+4
Session Chair(s): Yongfu Li (Shanghai Jiao Tong University, China), Yuhang Zhang (Shanghai Jiao Tong University, China), Yanan Sun (Shanghai Jiao Tong University, China), Yu Wu (University College London, UK), Bo Li (Xidian University, China)

4:30 pm – 6:30 pm
Student Design Competition Demo
SPECIAL EVENT

Venue: Leo 2+3+4
Session Chair(s): Kea-Tiong (Samuel) Tang (National Tsing Hua University, Taiwan), Elisabetta Moisello (University of Pavia)

4:30 pm – 6:30 pm
A4P-14 Circuit Techniques for ADC
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Qiang Li (University of Electronic Science and Technology)

ID1285: Digital Background Calibration Techniques for Interstage Gain Error and Nonlinearity in Pipelined ADCs
Qiao Wang (University of Electronic Science and Technology of China, China), Xizhu Peng (University of Electronic Science and Technology of China, China), Zhifei Lu (University of Electronic Science and Technology of China, China), Yutao Peng (University of Electronic Science and Technology of China, China), Zhe Hu (Chongqing Institute of Microelectronics Industry Technology, UESTC, China), He Tang (University of Electronic Science and Technology of China, China)

ID1875: A 4th Order CIFB High Dynamic Range Sigma-Delta Modulator with Multi-Level Quantizer and Intrinsically Linear Capacitive DACs

Haoyun Zhao (University of Edinburgh, United Kingdom), Xiongfei Jiang (University of Edinburgh, United Kingdom), Shiwei Wang (University of Edinburgh, United Kingdom)

ID1959: **Evolution Strategy and Controlled Residual Convolutional Neural Networks for ADC Calibration in the Absence of Ground Truth**
Zhe Hu (Chongqing Institute of Microelectronics Industry Technology, UESTC, China), Bowen Zhang (University of Electronic Science and Technology of China, China), He Tang (University of Electronic Science and Technology of China, China), Jia Pan (University of Hong Kong, Hong Kong), Xizhu Peng (University of Electronic Science and Technology of China, China)

ID2016: **A 16 GS/s Voltage-to-Time Conversion Sampler with 35.9 dB SNDR in 22 nm CMOS FDSOI**
Kai Misselwitz (Technische Universität Berlin, Germany), Friedel Gerfers (Technische Universität Berlin, Germany)

ID2335: **On the Segmentation of Gigasample Rate Current Steering DACs**
Antonio Aprile (University of Pavia, Italy), Edoardo Bonizzoni (University of Pavia, Italy), Piero Malcovati (University of Pavia, Italy)

4:30 pm – 6:30 pm
A4P-15 Reference & Regulators
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Yanhan Zeng (Guangzhou University)

ID1086: **A Chopper-Stabilized Bandgap Reference with a Double-Sampled FIR Filter in 180-nm CMOS**
Snehalatha Lalithamma (Indian Institute of Technology Roorkee, India), Saravana Kumar Manivannan (Indian Institute of Technology Roorkee, India)

ID1222: **A 1.02 ppm/°C Precision Bandgap Reference with High-Order Curvature Compensation for Fluorescence Detection**
Bingjun Xiong (Sun Yat-sen University, China), Feng Yan (Sun Yat-sen University, China), Wenji Mo (Sun Yat-sen University, China), Jian Guan (Sun Yat-sen University, China), Yuxuan Huang (Sun Yat-sen University, China), Jingjing Liu (Sun Yat-sen University, China)

ID1493: **A Wide Range Constant Transconductance Circuit Based on Negative Feedback for Analog Circuits**
Rakesh Kumar Palani (Indian Institute of Technology Delhi, India), Srishti Agrawal (Indian Institute of Technology Delhi, India), Ayan Alam Khan (Indian Institute of Technology Delhi, India), Aadarsh V (Indian Institute of Technology Delhi, India), Rajasekhar Nagulapalli (Oxford Brookes University, United Kingdom)

ID1850: **A Constant-Quiescent-Current and Fast-Transient CL-LDO with 99.99% Efficiency Using Dynamic Embedded Slew-Rate Enhancement Circuit**
Yue Wang (Shanghai University, China), Aiying Guo (Shanghai University, China), Jianhua Zhang (Shanghai University, China), Jingjing Liu (Shanghai University, China)

ID2072: **Compact Temperature Sensor with Voltage-Ratio Current-Independent Output for Reference Independent Data Conversion**
Kwabena Oppong Banahene (Iowa State University, United States), Randall Geiger (Iowa State University, United States)

4:30 pm – 6:30 pm
A4P-16 Digital Circuits, Systems & Architecture for Machine Learning V
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Bruce Sham (University of Auckland)

ID1448: A FPGA-Based Energy-Efficient Processor for Radar-Based Continuous Fall Detection
Juhua Chen (Shenzhen University, China), Linxin Yang (Shenzhen University, China), Wenbin Ye (Shenzhen University, China)

ID1487: A Method for Swift Selection of Appropriate Approximate Multipliers for CNN Hardware Accelerators
Peiyao Sun (University of Southampton, United Kingdom), Haosen Yu (University of Southampton, United Kingdom), Basel Halak (University of Southampton, United Kingdom), Tomasz Kazmierski (University of Southampton, United Kingdom)

ID1530: An FPGA-Based High-Throughput Dataflow Accelerator for Lightweight Neural Network
Zhiyuan Zhao (University of Science and Technology of China, China), Jixing Li (Institute of Semiconductors, Chinese Academy of Sciences, China), Gang Chen (Institute of Semiconductors, Chinese Academy of Sciences, China), Zhelong Jiang (Institute of Semiconductors, Chinese Academy of Sciences, China), Ruixiu Qiao (Institute of Semiconductors, Chinese Academy of Sciences, China), Peng Xu (Institute of Semiconductors, Chinese Academy of Sciences, China), Yihao Chen (Institute of Semiconductors, Chinese Academy of Sciences, China), Huaxiang Lu (Institute of Semiconductors, Chinese Academy of Sciences, China)

ID1043: DNNMapper: An Elastic Framework for Mapping DNNs to Multi-Die FPGAs
Shuyang Li (Fudan University, China), Xilang Zhou (Fudan University, China), Haodong Lu (Nanjing University of Posts and Telecommunications, China), Kun Wang (Fudan University, China)

ID1204: LauWS: Local Adaptive Unstructured Weight Sparsity of Load Balance for DNN in Near-Data Processing
Zixu Li (Fudan University, China), Wang Wang (Fudan University, China), Xin Zhong (Fudan University, China), Manni Li (Fudan University, China), Jiayu Yang (Fudan University, China), Yinyin Lin (Fudan University, China), Guhyun Kim (SK hynix Inc., Korea), Yosub Song (SK hynix Inc., Korea), Chengchen Wang (ZTE Corporation, China), Xiankui Xiong (ZTE Corporation, China)

4:30 pm – 6:30 pm
A4P-17 Digital Circuits, Systems & Architecture for Machine Learning VI
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Chung-An Shen (National Taiwan University of Science)

ID2203: An Energy-Efficient Differential Frame Convolutional Accelerator with On-Chip Fusion Storage Architecture and Pixel-Level Pipeline Data Flow
Zhenhui Dai (Peking University, China), Jiawei Wang (Peking University, China), Yi Zhong (Peking University, China), Kunyu Feng (Peking University, China), Cheng Zhao (Peking University, China), Yuanyuan Jiang (Peking University, China), Peiyu Chen (Peking University, China), Yuan Wang

(Peking University, China), Dunshan Yu (Peking University, China), Xiaoxin Cui (Peking University, China)

ID2228: **CINEMA: A Configurable Binary Segmentation Based Arithmetic Module for Mixed-Precision in-Memory Acceleration**
Runxi Wang (Shanghai Jiao Tong University, China), Ruge Xu (Shanghai Jiao Tong University, China), Xiaotian Zhao (Shanghai Jiao Tong University, China), Kai Jiang (Inspur Academy of Science and Technology, China), Xinfei Guo (Shanghai Jiao Tong University, China)

ID2242: **Low DRAM Memory Access and Flexible Dataflow Convolutional Neural Network Accelerator Based on RISC-V Custom Instruction**
Yi-Fan Chen (National Tsing Hua University, Taiwan), Yu-Jen Chang (National Tsing Hua University, Taiwan), Ching-Te Chiu (National Tsing Hua University, Taiwan), Ming-Long Huang (National Tsing Hua University, Taiwan), Geng-Ming Liang (National Tsing Hua University, Taiwan), Chao-Lin Lee (National Tsing Hua University, Taiwan), Jenq-Kuen Lee (National Tsing Hua University, Taiwan), Ping-Yu Hsieh (National Tsing Hua University, Taiwan), Wei-Chih Lai (MediaTek, Taiwan)

ID2278: **Accelerating Large-Scale DLRM Inference Through Dynamic Hot Data Rearrangement**
Taehyung Park (Seoul National University, Korea), Seungjin Yang (Seoul National University, Korea), Jongmin Seok (Inha University, Korea), Hyuk-Jae Lee (Seoul National University, Korea), Juhyun Kim (MetisX, Korea), Chae Eun Rhee (Inha University, Korea)

ID2314: **Energy Efficient Accurate and Approximate Modified Adders for Ternary Multipliers**
Hemanth L Krishna (Indian Institute of Technology Mandi, India), Nandit Kaushik (Indian Institute of Technology Mandi, India), Srinivasu Bodapati (Indian Institute of Technology Mandi, India)

5:00 pm – 6:30 pm
A5L-01 Analog Signal Processing I
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Aquarius 1
ORAL
Session Chair(s): Mohamad Sawan (Westlake University), Shahriar Mirabbasi (University of British Columbia)

5:00 pm
ID1233: **Gated Ring Oscillator Time Amplifier with Pico-Second Sensitivity and Applications in All-Digital Variable-Gain Time Integrator**
Fei Yuan (Toronto Metropolitan University, Canada)

5:18 pm
ID1996: **A Nanowatt Area-Efficient 16-Channel Bandpass Filterbank with Floating Active Capacitance Multiplier for Acoustic Signal Processing**
Zhongyi Zhang (Nanyang Technological University, Singapore), Wang Ling Goh (Nanyang Technological University, Singapore), Yuan Gao (Institute of Microelectronics, Agency for Science, Technology and Research, Singapore)

5:36 pm
ID2126: **Flip-Around Level-Shifting for Switched-Capacitor Amplifiers to Improve the Closed-Loop Settling of Floating-Inverter Amplifiers**
Ashwin Kumar Ramakrishnan Sivakumar (Indian Institute of Technology Kanpur, India)

5:54 pm
ID1049: **A 70dBA-460µW Companding Digital Silicon Microphone with Programmable Acoustic Overload Point and MEMS Asymmetry Robustness**
Jose Luis Ceballos (Infineon Technologies, Austria), Fulvio Ciciotti (Infineon Technologies, Austria), Christopher Rogi (Infineon Technologies, Austria), Alessandro Caspani (Infineon Technologies, Austria), Luca Sant (Infineon Technologies, Austria), Dietmar Straeussnigg (Infineon Technologies Austria, Austria), Andreas Wiesbauer (Infineon Technologies, Austria), Simon Gruenberger (Infineon Technologies, Austria), Chin Yeong Koh (Infineon Technologies, Singapore), Chern Sia Phillip Lim (Infineon Technologies, Singapore)

18:12 pm
ID1494: **A 23.8-Bit ENOB, ±5V Input Range Readout Circuit for High Precision Sensor Applications with 173.7dB-FoM**
Yinuo Chen (Fudan University, China), Lu Cao (Inbisen Semiconductor Co. Ltd., China), Hong Chen (Inbisen Semiconductor Co. Ltd., China), Liang Zou (Inbisen Semiconductor Co. Ltd., China), Cong Tang (Inbisen Semiconductor Co. Ltd., China), Junyu Wang (Fudan University, China)

5:00 pm – 6:30 pm
A5L-02 Sigma Delta Modulator for ADC
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Aquarius 2
ORAL
Session Chair(s): Jorge Fernandes (INESC-ID / Instituto Superior Técnico), Vishal Saxena (University of Delaware)

5:00 pm
ID2227: **A 99.8-dB SNDR 10kHz-BW Second-Order DT Delta-Sigma Modulator with Single OTA and Enhanced Noise-Coupling**
Jiaju Lu (Nanyang Technological University, Singapore), Siqi Zhang (Nanyang Technological University, Singapore), Wang Ling Goh (Nanyang Technological University, Singapore), Yuan Gao (Institute of Microelectronics, Agency for Science, Technology and Research, Singapore)

5:18 pm
ID1926: **A 172.5dB-FoM Hybrid CT/DT Incremental ΣΔ-Modulator for Direct Current-to-Digital Conversion**
Yinuo Chen (Fudan University, China), Liang Zou (Inbisen Semiconductor Co. Ltd., China), Cong Tang (Inbisen Semiconductor Co. Ltd., China), Hong Chen (Inbisen Semiconductor Co. Ltd., China), Junyu Wang (Fudan University, China)

5:36 pm
ID1753: **Offset Cancellation in Incremental ΔΣ ADCs**
Paul Kaesser (Universität Ulm, Germany), Omar Ismail (Universität Ulm, Egypt), David-Peter Wiens (Universität Ulm, Germany), Maurits Ortmanns (Universität Ulm, Germany)

17:54 pm
ID2090: **Using Negative-R Assisted Integrators in Wide-Band Delta-Sigma Modulators**
Ahmed Abdelaal (Universität Ulm, Germany), Michael Pietzko (Universität Ulm, Germany), Jonathan Ungethüm (Universität Ulm, Germany), John Kauffman (Universität Ulm, Germany), Maurits Ortmanns (Universität Ulm, Germany)

18:12 pm
ID1638: **A Sub-100 nW Power, Compact CTDSM with a Band-to-Band Tunnelling Loop Filter**

Atharva Raut (Indian Institute of Technology Bombay, India), Abhishek A. Kadam (Indian Institute of Technology Bombay, India), Ajay K. Singh (Indian Institute of Technology Bombay, India), Laxmeesha Somappa (Indian Institute of Technology Bombay, India), Maryam Shojaei Baghini (Indian Institute of Technology Bombay, India), Udayan Ganguly (Indian Institute of Technology Bombay, India)

5:00 pm – 6:30 pm
A5L-03 Low Power Logic, Circuits & Architectures II
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Aquarius 3
ORAL
Session Chair(s): Naeem Abbasi (Qualcomm), Tony Tae-Hyoung Kim (Nanyang Technological University)

5:00 pm
ID2581: **A Low-Power Single-Phase Split-Controlled Flip-Flop with No Redundant Switching**
Zhuoya Yan (Peking University, China), Yingna Huang (National University of Singapore, Singapore), Hailong Jiao (Peking University, China)

5:18 pm
ID1313: **Power-Efficient and Small-Area Approximate Multiplier Design with FPGA-Based Compressors**
Yi Guo (Yunnan University, China), Xiu Chen (Yunnan University, China), Qilin Zhou (Yunnan University, China), Heming Sun (Yokohama National University, Japan)

5:36 pm
ID2088: **An Energy-Efficient Object Detection System in IoT with Dynamic Neuromorphic Vision Sensors**
Zehao Li (Nanyang Technological University, Singapore), Wenhao Lu (Nanyang Technological University, Singapore), Yuncheng Lu (Nanyang Technological University, Singapore), Junying Li (Nanyang Technological University, Singapore), Yucen Shi (Nanyang Technological University, Singapore), Yuanjin Zheng (Nanyang Technological University, Singapore), Tony Tae-Hyoung Kim (Nanyang Technological University, Singapore)

5:54 pm
ID2443: **A Data-Distribution Aware Approximate Multiplier Design Based on FPGA**
Mingyu Shu (Tianjin University, China), Yingchang Mao (Tianjin University, China), Qiang Liu (Tianjin University, China)

6:12 pm
ID2020: **An FPGA-Based kNN Seach Accelerator for Point Cloud Registration**
Chengliang Wang (Chongqing University, China), Zhetong Huang (Chongqing University, China), Ao Ren (Chongqing University, China), Xun Zhang (Chongqing University, China)

5:00 pm – 6:30 pm
A5L-04 Digital Circuits, Systems & Architecture for Machine Learning II
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Aquarius 4
ORAL
Session Chair(s): Martinez Alonso Abdel (Tokyo Institute of Technology), Tian-Sheuan Chang (National Yang-Ming Chiao-Tung University)

5:00 pm
ID2163: A 3.55 mJ/Frame Energy-Efficient Mixed-Transformer Based Semantic Segmentation Accelerator for Mobile Devices
Jongjun Park (Korea Advanced Institute of Science and Technology, Korea), Seryeong Kim (Korea Advanced Institute of Science and Technology, Korea), Wonhoon Park (Korea Advanced Institute of Science and Technology, Korea), Seokchan Song (Korea Advanced Institute of Science and Technology, Korea), Hoi-Jun Yoo (Korea Advanced Institute of Science and Technology, Korea)

5:18 pm
ID2218: A 8.81 TFLOPS/W Deep-Reinforcement-Learning Accelerator with Delta-Based Weight Sharing and Block-Mantissa Reconfigurable PE Array (TCAS-II paper)
Sanghyuk An (Korea Advanced Institute of Science and Technology, Korea), Junha Ryu (Korea Advanced Institute of Science and Technology, Korea), Gwangtae Park (Korea Advanced Institute of Science and Technology, Korea), Hoi-Jun Yoo (Korea Advanced Institute of Science and Technology, Korea)

5:36 pm
ID1492: A 40nm 24.6TOPS/W Scalable EfficientDet Processor for Object Detection
Yu-Chuan Chuang (National Taiwan University, Taiwan), Ming-Guang Lin (National Taiwan University, Taiwan), Chi-Tse Huang (National Taiwan University, Taiwan), Chieh-Feng Teng (National Taiwan University, Taiwan), Cheng-Yang Chang (National Taiwan University, Taiwan), Yi-Ta Chen (National Taiwan University, Taiwan), An-Yeu Wu (National Taiwan University, Taiwan)

5:54 pm
ID1985: A 28nm Energy-Area-Efficient Row-Based Pipelined Training Accelerator with Mixed FXP4/FP16 for On-Device Transfer Learning
Wei Lu (National Yang Ming Chiao Tung University, Taiwan), Han-Hsiang Pei (National Yang Ming Chiao Tung University, Taiwan), Jheng-Rong Yu (National Yang Ming Chiao Tung University, Taiwan), Hung-Ming Chen (National Yang Ming Chiao Tung University, Taiwan), Po-Tsang Huang (National Yang Ming Chiao Tung University, Taiwan)

6:12 pm
ID2091: High Accuracy and Low Latency Mixed Precision Neural Network Acceleration for TinyML Applications on Resource-Constrained FPGAs
Wei Soon Ng (Nanyang Technological University, Singapore), Wang Ling Goh (Nanyang Technological University, Singapore), Yuan Gao (Institute of Microelectronics, Agency for Science, Technology and Research, Singapore)

5:00 pm – 6:30 pm
A5L-05 Cryptography & Hardware Security
TRACK 3: COMMUNICATIONS CIRCUITS AND SYSTEMS

Venue: Gemini 1
ORAL
Session Chair(s): Maire O'Neill (Queen's University Belfast), Dur-e-Shahwar Kundi (PQShield Ltd, UK)

5:00 pm
ID1057: Obfuscation of FSMs for Secure Outsourcing of Neural Network Inference Onto FPGAs
Rupesh Raj Karn (New York University, U.A.E.), Johann Knechtel (New York University, U.A.E.), Ozgur Sinanoglu (New York University, U.A.E.)

5:18 pm
ID1146: Interference Technology of Microphone Equipment Based on Time-Frequency Mosaic
Zichuan Yu (Southeast University, China), Lu Tang (Southeast University, China), Jianxun Li (Southeast University, China), Kai Wang (Southeast University, China), Yongchen Chen (Southeast University, China)

5:36 pm
ID1591: Efficient Soft Core Multiplier for Post Quantum Digital Signatures
Yasir Ali Shah (Queen's University Belfast, United Kingdom), Ciara Rafferty (Queen's University Belfast, United Kingdom), Ayesha Khalid (Queen's University Belfast, United Kingdom), Safiullah Khan (Manchester Metropolitan University, United Kingdom), Khalid Javeed (University of Sharjah, U.A.E.), Máire O'Neill (Queen's University Belfast, United Kingdom)

5:54 pm
ID1720: Compact 2^{17} NTT Architecture for Fully Homomorphic Encryption
Rella Mareta (Inha University, Korea), Hanho Lee (Inha University, Korea)

6:12 pm
ID2026: FPGA Bitstream Fault Injection Attack and Countermeasures on the Sampling Counter in CRYSTALS Kyber
Ziying Ni (Queen's University Belfast, United Kingdom), Ayesha Khalid (Queen's University Belfast, United Kingdom), Weiqiang Liu (Nanjing University of Aeronautics and Astronautics, China), Máire O'Neill (Queen's University Belfast, United Kingdom)

5:00 pm – 6:30 pm
A5L-06 Circuits & Systems for Wireless Power Transfer Applications
TRACK 4: POWER AND ENERGY CIRCUITS AND SYSTEMS

Venue: Gemini 2
ORAL
Session Chair(s): Chi-Seng Lam (University of Macau), Chi K. Tse (City University of Hong Kong)

5:00 pm
ID1406: Near-Field WPT System Design for Concurrent Charging of Two Independent Loads
Zhanel Kudaibergenova (Nazarbayev University, Kazakhstan), Kassen Dautov (Nazarbayev University, Kazakhstan), Mohammad Hashmi (Nazarbayev University, Kazakhstan)

5:18 pm
ID1531: A 6.78MHz Wireless Power Transfer System with Efficient Global Hysteresis Control for Implantable Medical Devices
Kai Cui (Northwestern Polytechnical University, China), Fantao Wang (Northwestern Polytechnical University, China), Ba Peng (Sichuan Changhong Battery Co., Ltd., China), Xiaoya Fan (Northwestern Polytechnical University, China), Yanzhao Ma (Northwestern Polytechnical University, China)

5:36 pm
ID2130: Design of Class-Φ3 Power Oscillator
Yutaro Komiyama (Chiba University, Japan), Wenqi Zhu (Chiba University, Japan), Akihiro Konishi (Chiba University, Japan), Kien Nguyen (Chiba University, Japan), Hiroo Sekiya (Chiba University, Japan)

5:54 pm
ID2222: **A 400 MHz Voltage-Mode-Based Fully Integrated Regulating Rectifier for Deep Tissue Bio-Implants**
Guoao Liu (Beihang University, China), Yuanqi Hu (Beihang University, China)

6:12 pm
ID2323: **Three Coils, High-Resolution Receiver Positioning System for Wireless Power Transfer**
Jiaxing Zhang (University College London, United Kingdom), Jiayang Li (University College London, United Kingdom), Dai Jiang (University College London, United Kingdom), Andreas Demosthenous (University College London, United Kingdom)

5:00 pm – 6:30 pm
A5L-07 Machine Learning & Signal Processing for Biomedical Systems I
TRACK 6: BIOMEDICAL CIRCUITS AND SYSTEMS

Venue: Pisces 1
ORAL
Session Chair(s): Xiao Liu (Fudan University, China), Jie Chen (University of Alberta, Edmonton, AB, Canada)

5:00 pm
ID1083: **An Ultra-Low Power Time-Domain Based SNN Processor for ECG Classification**
Haodong Fan (University of Electronic Science and Technology of China, China), Liang Chang (University of Electronic Science and Technology of China, China), Junlu Zhou (University of Electronic Science and Technology of China, China), Xi Yang (University of Electronic Science and Technology of China, China), Shuisheng Lin (University of Electronic Science and Technology of China, China), Jun Zhou (University of Electronic Science and Technology of China, China)

5:18 pm
ID1403: **An Ultra-Lightweight Time Period CNN Based Model with AI Accelerator Design for Arrhythmia Classification**
Shuenn-Yuh Lee (National Cheng Kung University, Taiwan), Wei-Cheng Tseng (National Cheng Kung University, Taiwan), Ju-Yi Chen (National Cheng Kung University Hospital, Taiwan)

5:36 pm
ID1606: **Hardware Implementation of a 16 Channel 0.16 µJ/Class Neural Tree for On-Chip Seizure Detection**
Anal Sharma (Indian Institute of Technology Bombay, India), Laxmeesha Somappa (Indian Institute of Technology Bombay, India)

5:54 pm
ID1810: **A Point Cloud-Based Non-Intrusive Approach for Human Posture Classification by Utilizing 77 GHz FMCW Radar and Deep Learning Models**
Pranjal Mahajan (International Institute of Information Technology Hyderabad, India), Devansh Chaudhary (Aligarh Muslim University, India), Mujeev Khan (Aligarh Muslim University, India), Mohammed Hammad Khan (International Institute of Information Technology Hyderabad, India), Mohd Wajid (Aligarh Muslim University, India), Abhishek Srivastava (International Institute of Information Technology Hyderabad, India)

6:12 pm
ID2433: **An Energy-Efficient Configurable Coprocessor Based on 1-D CNN for ECG Anomaly Detection**

Chen Zhang (Peking University, China), Zhijie Huang (Peking University, China), Qianxi Cheng (Peking University, China), Changchun Zhou (Peking University, China), Xin'An Wang (Peking University, China)

5:00 pm – 6:30 pm
A5L-08 Neural Learning Systems: Techniques & Applications I
TRACK 8: NEURAL NETWORKS AND NEUROMORPHIC ENGINEERING

Venue: Pisces 2
ORAL
Session Chair(s): Zhong Sun (Peking University), Li Yi (Huazhong University of Science and Technology)

5:00 pm
ID1663: GNeRF: Accelerating Neural Radiance Fields Inference via Adaptive Sample Gating
Cheng Gu (Shanghai Jiao Tong University, China), Gang Li (Shanghai Jiao Tong University, China), Xiaolong Lin (Shanghai Jiao Tong University, China), Jiayao Ling (Shanghai Jiao Tong University, China), Xiaoyao Liang (Shanghai Jiao Tong University, China)

5:18 pm
ID1379: A Reconfigurable Fused Multiply-Accumulate for Miscellaneous Operators in Deep Neural Network
Lei Lei (Beijing Institute of Technology, China), Zhiming Chen (Beijing Institute of Technology, China)

5:36 pm
ID1340: A Min-Max Optimization Framework for Multi-Task Deep Neural Network Compression
Jiacheng Guo (Cleveland State University, United States), Huiming Sun (Cleveland State University, United States), Minghai Qin (Western Digital Research, United States), Hongkai Yu (Cleveland State University, United States), Tianyun Zhang (Cleveland State University, United States)

5:54 pm
ID1503: An Attention Network with Self-Supervised Learning for Rheumatoid Arthritis Scoring
Deyu Ling (Southwest University of Science and Technology, China), Wenxin Yu (Southwest University of Science and Technology, China), Zhiqiang Zhang (Southwest University of Science and Technology, China), Jinmei Zou (Mianyang Central Hospital, China)

6:12 pm
ID1858: Decoupled Multi-Teacher Knowledge Distillation Based on Entropy
Xin Cheng (Hosei University, Japan), Jialiang Tang (Nanjing University of Science and Technology, China), Zhiqiang Zhang (Southwest University of Science and Technology, China), Wenxin Yu (Southwest University of Science and Technology, China), Ning Jiang (Southwest University of Science and Technology, China), Jinjia Zhou (Hosei University, Japan)

5:00 pm – 6:30 pm
A5L-09 Deep Learning for Visual Signal Representation & Processing
TRACK 11: VISUAL SIGNAL PROCESSING AND COMMUNICATIONS

Venue: Pisces 3
ORAL
Session Chair(s): Lap-Pui Chau (Hongkong Polytech Univ.), Zhu Li (Univ of Missouri, Kansas City)

5:00 pm
ID1241: An Iterative Image Inpainting Method Using Mask Shrinking
Haruka Matano (Hosei University, Japan), Haixin Wang (Hosei University, Japan), Jinjia Zhou (Hosei University, Japan)

5:18 pm
ID1282: Embedding Guide: Improving Watermarking Robustness and Imperceptibility Based on Attention and Edge Information
Baowei Wang (Nanjing University of Information Science and Technology, China), Xinyu Lv (Nanjing University of Information Science and Technology, China), Yufeng Wu (Nanjing University of Information Science and Technology, China), Changyu Dai (Nanjing University of Information Science and Technology, China), Zhengyu Hu (Nanjing University of Information Science and Technology, China), Xingyuan Zhao (Nanjing University of Information Science and Technology, China)

5:36 pm
ID1560: LATextSpotter: Empowering Transformer Decoder with Length Perception Ability
Zicheng Li (University of Science and Technology of China, China), Yadong Qu (University of Science and Technology of China, China), Hongtao Xie (University of Science and Technology of China, China), Yongdong Zhang (University of Science and Technology of China, China)

5:54 pm
ID1901: Depth-Powered Moving-Obstacle Segmentation Under Bird-Eye-View for Autonomous
Driving Shiyu Meng (Hong Kong Polytechnic University, China), Yi Wang (Hong Kong Polytechnic University, China), Lap-Pui Chau (Hong Kong Polytechnic University, China)

6:12 pm
ID2277: Video Assisted Face Recognition in Smart Classroom
Li-Wen Wang (Hong Kong Polytechnic University, Hong Kong), Wan-Chi Siu (Hong Kong Polytechnic University & Caritas Institute of Higher Education, Hong Kong), Yi-Hao Cheng (Hong Kong Polytechnic University, Hong Kong), H. Anthony Chan (Saint Francis University Hong Kong, Hong Kong)

5:00 pm – 6:30 pm
A5L-10 Optical & Wireless Communication & Sensing Technologies in Terrestrial & Non-Terrestrial Systems for 6G II
TRACK 14: SPECIAL SESSION

Venue: Pisces 4
ORAL
Session Chair(s): Shintaro Arai (Okayama University of Science), Di He (Shanghai Jiao Tong University)

5:00 pm
ID1016: Data Harvesting from Seabed-Mounted Observation Instruments Using Optical Wireless Communication on Underewater Drone
Takao Sawa (Japan Agency for Marine-Earth Science and Technology, Japan), Takeshi Nakatani (Japan Agency for Marine-Earth Science and Technology, Japan), Yosaku Maeda (Japan Agency for Marine-Earth Science and Technology, Japan), Tatsuya Asou (Japan Agency for Marine-Earth Science and Technology, Japan)

5:18 pm
ID1658: **Implementation of Robust Image Sensor Communication Using Light-Trail Surface by Rotating Propeller LED Transmitter**
Shintaro Arai (Okayama University of Science, Japan), Ryusei Nishimura (Okayama University of Science, Japan), Keisuke Yasui (Okayama University of Science, Japan), Daisuke Ito (Gifu University, Japan)

5:36 pm
ID1805: **GraSS: Graph Neural Networks for Loop Closure Detection with Semantic and Spatial Assistance**
Shihang Lu (University of Electronic Science and Technology of China, China), Zhuolin Peng (University of Electronic Science and Technology of China, China), Zhuoling Xiao (University of Electronic Science and Technology of China, China), Bo Yan (University of Electronic Science and Technology of China, China), Shuisheng Lin (University of Electronic Science and Technology of China, China), Sheng Yu (University of Electronic Science and Technology of China, China), Di He (Shanghai Jiao Tong University, China)

5:54 pm
ID2600: **Selective Multi-Pulse Pulse Position Modulation for Lighting Constrained Visible Light Communications**
Yusuke Kozawa (Ibaraki University, Japan)

5:00 pm – 6:30 pm
A5L-11 Improving Student Retention & Use of AI/ChatGPT in Engineering Education
TRACK 14: SPECIAL SESSION

Venue: Virgo 1
ORAL
Session Chair(s): Mohsin Jamali (University of Texas Permian Basin), Ljiljana Trajkovic (Simon Fraser University)

5:00 pm
ID1234: **Active Student Engagement in STEM Fields to Improve Retention and Graduation Rates**
Mohsin Jamali (University of Texas Permian Basin, United States), Sepehr Arbabi (University of Texas Permian Basin, United States), Hossein Hosseini (University of Texas Permian Basin, United States), Lokesh Saharan (University of Texas Permian Basin, United States)

5:18 pm
ID1286: **Early Impacts on Retention and Curriculum After Introducing a First-Year Experience**
CourseRussell Trafford (Rowan University, United States), Dwaipayan Chakraborty (Rowan University, United States), Ravi Ramachandran (Rowan University, United States)

5:36 pm
ID1289: **Enhanced Student-Graph Representation for At-Risk Student Detection**
Wei Qiu (Nanyang Technological University, Singapore), Andy W. H. Khong (Nanyang Technological University, Singapore), Fun Siong Lim (Nanyang Technological University, Singapore)

5:54 pm
ID1586: **Prospectives on the Use of ChatGPT in Education: Pros and Cons with a Classical Approach**
Gordana Jovanovic Dolecek (National Institute of Astrophysics, Optics and Electronics, Mexico), Andres Rojas (National Institute of Astrophysics, Optics and Electronics, Mexico)

6:12 pm
ID1640: Exploration of Generative AI Tools for an Electric Circuits Course
Tokunbo Ogunfunmi (Santa Clara University, United States)

5:00 pm – 6:30 pm
A5L-12 Various Synchronization in Coupled Nonlinear Circuits with Specialized Coupling & Applications
TRACK 14: SPECIAL SESSION

Venue: Virgo 2
ORAL
Session Chair(s): Yoko Uwate (Tokushima University), Tadashi Tsubone (Nagaoka University of Technology)

5:00 pm
ID2137: Synchronizations in Oscillatory Networks with Memristor Couplings as Ring Structure
Yukinojo Kotani (Tokushima University, Japan), Yoko Uwate (Tokushima University, Japan), Yoshifumi Nishio (Tokushima University, Japan)

5:18 pm
ID2364: Synchronization Phenomena in Coupled Impact Oscillator Model of Rocking Robots on a Suspension Bridge
Yuta Togashi (Nagaoka University of Technology, Japan), Tadashi Tsubone (Nagaoka University of Technology, Japan)

5:36 pm
ID2298: Development of an Initial Value Input System for a Ring of Coupled Four Oscillators
Fumito Shinomiya (Hiroshima Institute of Technology, Japan), Masayuki Yamauchi (Hiroshima Institute of Technology, Japan)

5:54 pm
ID1872: Spectral Mode Decomposition of Propagating Wave in Five-Coupled Bistable Oscillators
Kuniyasu Shimizu (Chiba Institute of Technology, Japan)

6:12 pm
ID1928: Behavior of Phase-Inversion Waves on Coupled Van der Pol Oscillators as a Torus
Kyosuke Yasuda (Hiroshima Institute of Technology, Japan), Masayuki Yamauchi (Hiroshima Institute of Technology, Japan)

5:00 pm – 6:30 pm
A5L-13 AI-Based Detection & Estimation for Health & Security Applications
TRACK 14: SPECIAL SESSION

Venue: Virgo 3
ORAL
Session Chair(s): Wei Liu (Queens Mary University of London), Yudong Zhang (University of Leicester)

5:00 pm
ID1632: Deep Learning Based Source Direction Estimation with Magnitude-Only Array Measurements

Jingdong Kuang (Queen Mary University of London, United Kingdom), Wei Liu (Queen Mary University of London, United Kingdom), Zhengyu Wan (Shenzhen MSU-BIT University, China)

5:18 pm
ID2604: Machine Learning for X-Ray and CT-Based COVID-19 Diagnosis
Min Tang (Jiangsu Second Normal University, China), Shuwen Chen (Southeast University, China), Shuihua Wang (University of Leicester, United Kingdom), Yudong Zhang (University of Leicester, United Kingdom)

5:36 pm
ID2024: P2E-LGAN: PPG to ECG Reconstruction Methodology Using LSTM Based Generative Adversarial Network
Rashmi Kumari (Indian Institute of Technology Hyderabad, India), Surita Sarkar (Indian Institute of Technology Hyderabad, India), Debeshi Dutta (Indian Institute of Technology Hyderabad, India), Pabitra Das (Indian Institute of Technology Hyderabad, India), Amit Acharyya (Indian Institute of Technology Hyderabad, India)

5:54 pm
ID2094: Code Property Graph Based Cross-Domain Vulnerability Detection via Deep Fused Feature
Gewangzi Du (Chinese Academy of Sciences, China), Liwei Chen (Chinese Academy of Sciences, China), Tongshuai Wu (Chinese Academy of Sciences, China), Xiong Zheng (Chinese Academy of Sciences, China), Gang Shi (Chinese Academy of Sciences, China)

6:12 pm
ID2525: Machine Learning for Monitoring Vocal Health and Performance of Professional Singers
Samuel Jones (University of Westminster, United Kingdom), Saumya Reni (University of Westminster, United Kingdom), Izzet Kale (University of Westminster, United Kingdom)

6:30 pm – 9:00 pm
WiCAS-YPCAS Event
SPECIAL EVENT

Venue: Leo 1
Panellists: Yao Zhu (Institute of Microelectronics), Marcus Janke (Infineon Technologies AG Munich), Chi-Seng Lam (University of Macau), Yi (Estelle) Wang (Continental Automotive)
Moderator: Eugene Seah (Abundance Life Coach)

Technical Program: Tuesday 21 May 2024

7:45 am – 8:30 am
Registration
Venue: Foyer of Taurus Room (Secretariat Room)

8:30 am – 10:00 am
PhD Forum (Oral)
SPECIAL EVENT

Venue: Pisces 3
Session Chair(s): Yongfu Li (Shanghai Jiao Tong University, China), Yuhang Zhang (Shanghai Jiao Tong University, China), Yanan Sun (Shanghai Jiao Tong University, China), Yu Wu (University College London, UK), Bo Li (Xidian University, China)

8:30 am – 10:00 am
Info Security Part 1
EMBEDDED WORKSHOP

Venue: Leo 1
Session Chair(s): Dr. Shivam Bhasin (NTU, Singapore)

8:30 am – 10:00 am
SW: CAS Standard Workshop on Digital Healthcare I
SPECIAL WORKSHOP

Venue: Virgo 4
Session Chair(s): Yongfu Li (Shanghai Jiao Tong University, China), Boon Chong Ang (Intel), Yang Zhao (Shanghai Jiao Tong University, China), Wei Mao (Xidian University, China), and Lian Yong (York University)

8:30 am – 10:00 am
B2L-01 Fractional N & All Digital PLL
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Aquarius 1
ORAL
Session Chair(s): Hui Wang (Shanghai Jiao Tong University), Robert Sobot (University of Western Ontario)

08:30 am
ID2146: A Fractional-N PLL for Multi-Phase Clock Generation with Loop Bandwidth Enhancement
Reo Nagasue (Toyama Prefectural University, Japan), Isamu Mizuno (Toyama Prefectural University, Japan), Ryo Kishida (Toyama Prefectural University, Japan), Tatsuya Iwata (Toyama Prefectural University, Japan), Takefumi Yoshikawa (Toyama Prefectural University, Japan)

08:48 am
ID2223: A Bang-Bang All-Digital Phase-Locked Loop with an Implicit Common-Mode Resonant Oscillator
Ruixu Wang (Peking University, China)

09:06 am
ID1639: A Reduced-Fractional-Spur DPLL Based on Cyclic Single-Delay-Pair Vernier TDC
Ping Lu (Microsoft, United States), Minhan Chen (Microsoft, United States), Shaishav Desai (Microsoft, United States)

09:24 am
ID1520: Fractional-N Injection-Locked Ring Oscillator Based on Two Points, Varying Strength Injection
Xu Meng (Hefei University of Technology, China), Jinxia Geng (Hefei University of Technology, China), Xu Tang (Hefei University of Technology, China), Min Zhou (Hefei University of Technology, China), Hailin Teng (Hefei University of Technology, China)

09:42 am
ID2127: A Low In-Band Phase Noise Fractional-N ADPLL Based on Switched-Capacitor-DPI
Ningyuan Zhang (Peking University, China), Sihao Zhang (Peking University, China), Junhua Liu (Peking University, China), Huailin Liao (Peking University, China)

8:30 am – 10:00 am
B2L-02 ADC/DAC Circuits
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Aquarius 2
ORAL
Session Chair(s): Ankesh Jain, Jose de la Rosa

08:30 am
ID1011: A 600MS/s 10-Bit SAR ADC with Unit Via-Based Delta-Length C-DAC in 22nm FDSOI
Michael Pietzko (Universität Ulm, Germany), Jonathan Ungethüm (Universität Ulm, Germany), Ahmed Abdelaal (Universität Ulm, Germany), John Kauffman (Universität Ulm, Germany), Maurits Ortmanns (Universität Ulm, Germany)

08:48 am
ID1472: Low-Cost Linearity Testing of High-Resolution ADCs Using Segmentation Modeling and Partial Polynomial Fitting
Dengquan Li (Xidian University, China), Yexin Zhu (Xidian University, China), Longsheng Wang (Xidian University, China), Shubin Liu (Xidian University, China), Zhangming Zhu (Xidian University, China)

09:06 am
ID1478: A 14-Bit 6GS/s DAC Achieving >65dBc SFDR with Bilateral Output Impedance Compensation in 22nm CMOS
Xinpeng Xing (Sun Yat-sen University, China), Qiji Huang (Tsinghua University, China), Tinghua Chen (Tsinghua University, China), Haigang Feng (Tsinghua University, China), Zhongfeng Wang (Sun Yat-sen University, China)

09:24 am
ID2193: A 10b 400MS/s 2x-Time-Interleaved 2-Then-1b/Cycle SAR ADC in 90nm CMOS
Wei-Chung Lin (National Taiwan University of Science and Technology, Taiwan), Yung-Chi Chang (National Taiwan University of Science and Technology, Taiwan), Yung-Hui Chung (National Taiwan University of Science and Technology, Taiwan)

09:42 am
ID1030: An Easy-to-Drive Discrete-Time ADC Topology Using Digital Predictive Level-Shifting
Manxin Li (Oregon State University, United States), Runpeng Gao (Oregon State University, United States), Calder Wilson (Oregon State University, United States), Amartya Basak (Oregon State University, United States), Evan Markwell (Oregon State University, United States), Matthew Johnston (Oregon State University, United States), Un-Ku Moon (Oregon State University, United States)

8:30 am – 10:00 am
B2L-03 Advanced Memory & Computing-in-Memory Circuits I
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Aquarius 3
ORAL
Session Chair(s): Anh Tuan Do (IME ASTAR), Tian-Sheuan Chang (National Yang-Ming Chiao-Tung University)

08:30 am
ID1326: AFT-CIM: An Energy Efficient ADC-Free Transpose Computing-in-Memory Macro for MAC Operations
Shuai Wang (University of Science and Technology of China, China), Yuang Ma (University of Science and Technology of China, China), Yi Kang (University of Science and Technology of China, China)

08:48 am
ID1642: A Mixed-Signal Compute-in-Memory Architecture for Solving All-to-All Connected MAXCUT Problems with Sub-µs Time-to-Solution
Alana Dee (University of Washington, United States), Katherine Bennett (Grove City College, United States), Sajjad Moazeni (University of Washington, United States)

09:06 am
ID1321: Trident-CIM: A LUT-Based Compute-in-Memory Macro with Trident Read Bit-Line and Partial Product Pruning (TCAS-II paper)
Hongyi Zhang (Fudan University, China), Siqi He (Fudan University, China), Mengjie Li (Fudan University, China), Haozhe Zhu (Fudan University, China), Chengchen Wang (ZTE Corporation, China), Xiankui Xiong (ZTE Corporation, China), Haidong Tian (State Key Laboratory of Mobile Network and Mobile Multimedia Technology, ZTE Corporation, China), Xiaoyang Zeng (Fudan University, China), Chixiao Chen (Fudan University, China)

09:24 am
ID1953: An eDRAM Based Computing-in-Memory Macro with Full-Valid-Storage and Channel-Wise-Parallelism for Depthwise Neural Network (TCAS-II paper)
Xin Qiao (Peking University, China), Youming Yang (Peking University, China), Chang Xue (Peking University, China), Yandong He (Peking University, China), Xiaoxin Cui (Peking University, China), Song Jia (Peking University, China), Yuan Wang (Peking University, China)

09:42 am
ID1958: A 2T P-Channel Logic Flash Cell for Reconfigurable Interconnection in Chiplet-Based Computing-in-Memory Accelerators
Weizeng Li (Institute of Microelectronics Chinese Academy of Sciences, University of Chinese Academy of Sciences, China), Linfang Wang (Institute of Microelectronics Chinese Academy of Sciences, University of Chinese Academy of Sciences, China), Zhi Li (Institute of Microelectronics Chinese Academy of Sciences, University of Chinese Academy of Sciences, China), Wang Ye

(Institute of Microelectronics Chinese Academy of Sciences, University of Chinese Academy of Sciences, China), Zhidao Zhou (Institute of Microelectronics Chinese Academy of Sciences, University of Chinese Academy of Sciences, China), Haiyang Zhou (Institute of Microelectronics Chinese Academy of Sciences, University of Chinese Academy of Sciences, China), Hanghang Gao (Institute of Microelectronics Chinese Academy of Sciences, University of Chinese Academy of Sciences, China), Jinshan Yue (Institute of Microelectronics Chinese Academy of Sciences, China), Hongyang Hu (Institute of Microelectronics Chinese Academy of Sciences, China), Fengman Liu (Institute of Microelectronics Chinese Academy of Sciences, China), Qing Luo (Institute of Microelectronics Chinese Academy of Sciences, China), Chunmeng Dou (Institute of Microelectronics Chinese Academy of Sciences, China)

8:30 am – 10:00 am
B2L-04 Digital Circuits, Systems & Architecture for Machine Learning III
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Aquarius 4
ORAL
Session Chair(s): Yeong-Kang Lai (National Chung Hsing University), Bruce Sham (University of Auckland)

08:30 am
ID1120: An FPGA-Based Accelerator Enabling Efficient Support for CNNs with Arbitrary Kernel Sizes
Miaoxin Wang (Nanjing University, China), Xiao Wu (Nanjing University, China), Jun Lin (Nanjing University, China), Zhongfeng Wang (Nanjing University, China)

08:48 am
ID1067: PBN: Progressive Batch Normalization for DNN Training on Edge Device
Yingchang Mao (Tianjin University, China), Mingyu Shu (Tianjin University, China), Qiang Liu (Tianjin University, China)

09:06 am
ID1876: A Flexible FPGA-Based Accelerator for Efficient Inference of Multi-Precision CNNs
Xinyan Liu (Nanjing University, China), Xiao Wu (Nanjing University, China), Haikuo Shao (Nanjing University, China), Zhongfeng Wang (Nanjing University, China)

09:24 am
ID1768: HeNCoG: A Heterogeneous Near-Memory Computing Architecture for Energy Efficient GCN Acceleration
Seung-Eon Hwang (Korea University, Korea), Duyeong Song (Korea University, Korea), Jongsun Park (Korea University, Korea)

09:42 am
ID2115: A 422.1 Mpixels/J Tile-Based 4K Super Resolution Processor with Variable Bit Compression
Wuyoung Jang (Ulsan National Institute of Science and Technology, Korea), Sangho Lee (Ulsan National Institute of Science and Technology, Korea), Jinhoon Jo (Ulsan National Institute of Science and Technology, Korea), Jueun Jung (Ulsan National Institute of Science and Technology, Korea), Donghyeon Han (Massachusetts Institute of Technology, United States), Kyuho Lee (Ulsan National Institute of Science and Technology, Korea)

8:30 am – 10:00 am
B2L-05 Wireless Communications I

TRACK 3: COMMUNICATIONS CIRCUITS AND SYSTEMS

Gemini 1
ORAL
Session Chair(s): Jiafeng Xie (Villanova University)

08:30 am
ID1716: A 2.4GHz Sub-Passive RF Down-Converter with Trans-Frequency Current-Reusing Scheme Achieving Low Flicker Noise and High Linearity
Yan Zhao (Southeast University, China), Chao Chen (Southeast University, China), Wenjing Zhang (Southeast University, China), Jun Yang (Southeast University, China)

08:48 am
ID2069: FLAG: Formula-LLM-Based Auto-Generator for Baseband Hardware
Yunwei Mao (Southeast University, China), You You (Southeast University, China), Xiaosi Tan (Southeast University, China), Yongming Huang (Southeast University, China), Xiaohu You (Southeast University, China), Chuan Zhang (Southeast University, China)

09:06 am
ID2181: A 825 MHz 2.83 µW −70 dBm Sensitivity Wake-Up Receiver with Resonant Noise Matching
Qinghao Liu (Nanyang Technological University, Singapore), Chuanshi Yang (Virtus IC Design Center of Excellence, Nanyang Technological University, Singapore), Yange Wang (Nanyang Technological University, Singapore), Chun Huat Heng (National University of Singapore, Singapore), Yuanjin Zheng (Nanyang Technological University, Singapore)

09:24 am
ID1267: A Novel Low-Complexity Massive MIMO Detector with Near-Optimum Performance
Jinjie Hu (Nanjing University, China), Suwen Song (Sun Yat-sen University, China), Zhongfeng Wang (Nanjing University, China)

09:42 am
ID2046: Massive MIMO Signal Detection Using SRAM-Based In-Memory Computing
Mihir Kavishwar (University of Illinois Urbana-Champaign, United States), Naresh Shanbhag (University of Illinois Urbana-Champaign, United States)

8:30 am – 10:00 am
B2L-06 Modeling & Control of Power & Energy Circuits & Systems
TRACK 4: POWER AND ENERGY CIRCUITS AND SYSTEMS

Venue: Gemini 2
ORAL
Session Chair(s): Hirro Sekiya (Chiba University), Giulia Di Capua (University of Cassino and Southern Lazio)

08:30 am
ID1358: A Generalized Harmonic Injection Analysis Aimed at Improving Power Transfer (TCAS-II paper)
Alvaro Volpato (University of São Paulo, Brazil), Luis Alberto (University of São Paulo, Brazil), Ricardo Machado (University of São Paulo, Brazil)

08:48 am
ID1305: A Steady-State Operation Based Online Parameter Identification Method of Output Capacitor for DC-DC Buck Converters

Chio-Hong Leong (University of Macau, Macau), Chi-Kong Wong (University of Macau, Macau), Cheng Gong (University of Macau, Macau), Chi-Seng Lam (University of Macau, Macau)

09:06 am
ID2388: **A Programmable and Adaptive Dead-Time Controller for Low-Offset Output Generation for Cryo-Cooler Drive Applications**
Nishant Kumar (Indian Institute of Technology Gandhinagar, India), Hari Shanker Gupta (Space Applications Centre, India), Anuj Srivastava (Space Applications Centre, India), Nihar Ranjan Mohapatra (Indian Institute of Technology Gandhinagar, India)

09:24 am
ID1246: **Finite Set Model Predictive Control for PWM Rectifiers Based on Data-Driven Neural Network Predictor**
Lu Liu (Dalian Maritime University, China), Tao Shi (Dalian Maritime University, China), Dan Wang (Dalian Maritime University, China), Nan Gu (Dalian Maritime University, China), Zhouhua Peng (Dalian Maritime University, China)

09:42 am
ID1274: **Prediction of Subharmonic Oscillation in SIMO DC-DC Converter with Ordered Power Distributive Control in CCM and Peak Current Mode**
Zhewen Yu (University of Macau, China), Fangyu Mao (University of Macau, China), Yan Lu (University of Macau, China)

8:30 am – 10:00 am
B2L-07 Multimedia Systems for Coding & Processing
TRACK 12: MULTIMEDIA SYSTEMS AND APPLICATIONS

Venue: Pisces 1
ORAL
Session Chair(s): Jiaying Liu (Peking University), Li Li (University of Science and Technology of China)

08:30 am
ID1134: **Content-Adaptive Variable Resolution Framework for Intra Coding**
Jiyu Xie (University of Science and Technology of China, China), Li Li (University of Science and Technology of China, China), Dong Liu (University of Science and Technology of China, China), Houqiang Li (University of Science and Technology of China, China)

08:48 am
ID1582: **Rate Control for Slimmable Video Codec Using Multilayer Perceptron**
Defa Wang (Northwestern Polytechnical University, China), Zhiwei Zhu (Northwestern Polytechnical University, China), Shuai Wan (Northwestern Polytechnical University, China), Fei Yang (Computer Vision Center, Universitat Autonoma de Barcelona, Spain), Luis Herranz (Computer Vision Center, Universitat Autonoma de Barcelona, Spain)

09:06 am
ID1141: **Enhancing Real-Time Video Streaming with Joint Frame Size and Rate Adaptation**
Hengchao Wang (Shanghai Jiao Tong University, China), Ziyu Zhong (Shanghai Jiao Tong University, China), Jiaoyang Yin (Shanghai Jiao Tong University, China), Yiling Xu (Shanghai Jiao Tong University, China), Le Yang (University of Canterbury, New Zealand)

09:24 am
ID1254: **Improving Optimal Binarization with Update On-the-Fly in G-PCC Entropy Coding: Probability Initialization and Adaptive Bounds Setting for Context Models**

Shidi Hao (Northwestern Polytechnical University, China), Shuai Wan (Northwestern Polytechnical University, China), Tengya Tian (Xidian University, China), Wei Zhang (Xidian University, China), Fuzheng Yang (Xidian University, China)

09:42 am
ID2360: **RDLNET: Residual Dense Block Based Lightweight Network for Video Super-Resolution**
Kuan-Hsien Liu (National Taichung University of Science and Technology, Taiwan), Chih-Jung Wang (National Taichung University of Science and Technology, Taiwan), Tsung-Jung Liu (National Chung Hsing University, Taiwan), Wen-Ren Liu (National Taichung University of Science and Technology, Taiwan)

8:30 am – 10:00 am
B2L-08 Neuromorphic Spiking Learning Systems & Applications I
TRACK 8: NEURAL NETWORKS AND NEUROMORPHIC ENGINEERING

Venue: Pisces 2
ORAL
Session Chair(s): Mostafa Rahimi Azghadi (James Cook University), Zhuo Zou (Fudan University)

08:30 am
ID1729: **A 0.96pJ/SOP, 30.23K-neuron/mm² Heterogeneous Neuromorphic Chip with Fullerene-Like Interconnection Topology for Edge-AI Computing**
Pujun Zhou (University of Electronic Science and Technology of China, China), Qi Yu (University of Electronic Science and Technology of China, China), Ming Chen (University of Electronic Science and Technology of China, China), Yuchen Wang (University of Electronic Science and Technology of China, China), Liwei Meng (University of Electronic Science and Technology of China, China), Yue Zuo (University of Electronic Science and Technology of China, China), Ning Ning (University of Electronic Science and Technology of China, China), Yang Liu (University of Electronic Science and Technology of China, China), Shaogang Hu (University of Electronic Science and Technology of China, China), Guanchao Qiao (University of Electronic Science and Technology of China, China)

08:48 am
ID2522: **A Fully-Parallel Reconfigurable Spiking Neural Network Accelerator with Structured Sparse Connections**
Mingyang Li (Nara Institute of Science and Technology, Japan), Yirong Kan (Nara Institute of Science and Technology, Japan), Renyuan Zhang (Nara Institute of Science and Technology, Japan), Yasuhiko Nakashima (Nara Institute of Science and Technology, Japan)

09:06 am
ID1018: **A Reduced Spiking Neural Network Architecture for Energy Efficient Context-Dependent Reinforcement Learning Tasks**
Hira Rasheed (Oslo Metropolitan University, Norway), Peyman Mirtaheri (Oslo Metropolitan University, Norway), Ali Muhtaroglu (Oslo Metropolitan University, Norway)

09:24 am
ID1483: **A Compact Low Power Multi-Mode Spiking Neuron Using Band to Band Tunneling**
Abhishek A. Kadam (Indian Institute of Technology Bombay, India), Ajay K. Singh (Indian Institute of Technology Bombay, India), Laxmeesha Somappa (Indian Institute of Technology Bombay, India), Maryam Shojaei Baghini (Indian Institute of Technology Bombay, India), Udayan Ganguly (Indian Institute of Technology Bombay, India)

09:42 am
ID2590: [AnSpiCS-Net: Reconfigurable Network-on-Chip for Analog Spiking Recurrent Neural Networks]
Manu Rathore (University of Tennessee, United States), Garrett S. Rose (University of Tennessee, United States)

8:30 am – 10:00 am
B2L-10 Compact Smart Wearable Devices & Digital Health
TRACK 14: SPECIAL SESSION

Venue: Pisces 4
ORAL
Session Chair(s): Guoxing Wang (Shanghai Jiao Tong Univ, China), Yao Wang (Chinese University of Hong Kong)

08:30 am
ID2464: [A Transformer-Based Deep Learning Model for Sleep Apnea Detection and Application on RingConn Smart Ring]
Zetong Wu (Shenzhen University, China), Hao Wu (Shenzhen University, RingConn LLC, China), Kaiqun Fang (Shenzhen University, China), Keith Siu-Fung Sze (RingConn LLC, United States), Qianjin Feng (RingConn LLC, United States)

08:48 am
ID2406: [Non-Invasive Continuous Real-Time Blood Glucose Estimation Using PPG Features-Based Convolutional Autoencoder with TinyML Implementation]
Noor Faris Ali (United Arab Emirates University, U.A.E.), Alyazia Aldhaheri (United Arab Emirates University, U.A.E.), Bethel Wodajo (United Arab Emirates University, U.A.E.), Meera Alshamsi (United Arab Emirates University, U.A.E.), Shaikha Alshamsi (United Arab Emirates University, U.A.E.), Mohamed Atef (United Arab Emirates University, U.A.E.)

09:06 am
ID2463: [A Frequency-Domain Features Based Clustering Algorithm for Blood Pressure Estimation with Photoplethysmogram Signal]
Ruifang Liu (Shenzhen University, China), Shijie Cheng (Shenzhen University, China), Hao Wu (Shenzhen University, RingConn LLC, China), Keith Siu-Fung Sze (RingConn LLC, United States), Qianjin Feng (RingConn LLC, United States)

09:24 am
ID2479: [A Low-Noise, Low-Power Neural Signal Amplifier for Deep Brain Stimulation System Chips Tolerating 3V Stimulation]
Chia-Hua Hsu (National Tsing Hua University, Taiwan), Yu-Wei Lin (National Tsing Hua University, Taiwan), Kea-Tiong Tang (National Tsing Hua University, Taiwan)

09:42 am
ID2509: [BOLS: A Bionic Sensor-Direct On-Chip Learning System with Direct-Feedback-Through-Time for Personalized Wearable Health Monitoring]
Fengshi Tian (Hong Kong University of Science and Technology, Hong Kong), Jiakun Zheng (Hong Kong University of Science and Technology, Hong Kong), Jingyu He (Hong Kong University of Science and Technology, Hong Kong), Jinbo Chen (Westlake University & Zhejiang University, China), Xiaomeng Wang (Hong Kong University of Science and Technology, Hong Kong), Chaoming Fang (Westlake University, China), Jie Yang (Westlake University, China), Mohamad Sawan (Westlake University, China), Chi-Ying Tsui (Hong Kong University of Science and Technology, Hong Kong), Kwang-Ting Cheng (Hong Kong University of Science and Technology, Hong Kong)

8:30 am – 10:00 am
B2L-11 Grand Challenge on Neural Network-based Video Coding
TRACK 14: SPECIAL SESSION

Venue: Virgo 1
ORAL
Session Chair(s): Li Zhang (Bytedance Inc.), Kai Zhang (Bytedance Inc.)

08:30 am
ID1802: Privacy-Preserving with Flexible Autoencoder for Video Coding for Machines
Aorui Gou (Fudan University, China), Heming Sun (Yokohama National University, Japan), Xiaoyang Zeng (Fudan University, China), Yibo Fan (Fudan University, China)

08:48 am
ID2219: Geometry Transform of Intra-Frames in ECM
Wei Jia (ByteDance Inc., United States), Kai Zhang (ByteDance Inc., United States), Yang Wang (ByteDance Inc., United States), Tianliang Fu (ByteDance Inc., United States), Yue Li (ByteDance Inc., United States), Li Zhang (ByteDance Inc., United States)

09:06 am
ID2224: Conditional Variational Autoencoders for Hierarchical B-Frame Coding
Zong-Lin Gao (National Yang Ming Chiao Tung University, Taiwan), Cheng-Wei Chen (National Yang Ming Chiao Tung University, Taiwan), Yi-Chen Yao (National Yang Ming Chiao Tung University, Taiwan), Cheng-Yuan Ho (National Yang Ming Chiao Tung University, Taiwan), Wen-Hsiao Peng (National Yang Ming Chiao Tung University, Taiwan)

09:24 am
ID2488: VQNeRV: Vector Quantization Neural Representation for Video Compression
Gai Zhang (University of the Chinese Academy of Sciences, China), Lv Tang (University of the Chinese Academy of Sciences, China), Xinfeng Zhang (University of Chinese Academy of Sciences, China)

8:30 am – 10:00 am
B2L-12 12th International Workshop on Computational Intelligence for Multimedia Understanding
TRACK 16: 12TH INTERNATIONAL WORKSHOP ON COMPUTATIONAL INTELLIGENCE FOR MULTIMEDIA UNDERSTANDING

Venue: Virgo 2
ORAL
Session Chair(s): Maria Trocan (ISEP), Behçet Uğur Töreyin (Informatics Institute, Istanbul Technical University)

08:30 am
ID1288: Performance Study by Changing the Internal Structure of Hysteresis Reservoir Computing
Kenta Yokoyama (Tokyo City University, Japan), Kenya Jin'no (Tokyo City University, Japan)

08:48 am
ID2112: Examination of the Relationship Between Feature Extraction by Kernels and CNN
Performance Sora Togawa (Tokyo City University, Japan), Kenya Jin'no (Tokyo City University, Japan)

09:06 am
ID2608: **A Multi-Farm Irrigation Scheduling System (MISS) for Arid and Semi-Arid Regions: A Realistic Scenario**
Dalhatu Muhammed (Institut Supérieur d'Electronique de Paris, France), Ehsan Ahvar (Nokia Networks Massy, France), Shohreh Ahvar (Nokia Networks Massy, France), Maria Trocan (Institut Supérieur d'Electronique de Paris, France), Reza Ehsani (University of California, Merced, United States)

09:24 am
ID2609: **Generated Compressed Domain Images to the Rescue: Cross Distillation from Compressed Domain to Pixel Domain**
Reyhan Kevser Keser (Istanbul Technical University, Turkey), Muhammet Sebul Beratoğlu (Istanbul Technical University, Turkey), Behçet Uğur Töreyin (Istanbul Technical University, Turkey)

09:42 am
ID2610: **Design and Implementation of Optical Fiber-Based Visible Light Communication System**
Zixuan Ling (Nanchang University, China), Xuanbang Chen (Nanchang University, China), Yuhao Wang (Nanchang University, China), Xun Zhang (Institut Supérieur d'Electronique de Paris, France), Xiaodong Liu (Nanchang University, China), Zhenghai Wang (Nanchang University, China)

8:30 am – 10:00 am
B2L-13 Trustable & Sustainable Intelligent Circuits & System Design
TRACK 14: SPECIAL SESSION

Venue: Virgo 3
ORAL
Session Chair(s): Kun-Chih - Jimmy Chen (National Yang Ming Chiao Tung University), Trevor E. Carlson (National University of Singapore)

08:30 am
ID2000: **Enhancing Stability in CRPs: A Novel Parallel Scan-Chain PUF Design Considering Aging Effects**
Yu-Guang Chen (National Central University, Taiwan), Tzong-Ying Lee (National Central University, Taiwan), Yi-Ting Lin (National Central University, Taiwan)

08:48 am
ID1906: **Design Flow for Incorporating Camouflaged Logic Gates to Enhance Hardware Security While Considering Timing Closure**
Liang-Ying Su (Chung Yuan Christian University, Taiwan), Shih-Hsu Huang (Chung Yuan Christian University, Taiwan)

09:06 am
ID1168: **Hardware Accelerator for MobileViT Vision Transformer with Reconfigurable Computation**
Shen-Fu Hsiao (National Sun Yat-sen University, Taiwan), Tzu-Hsien Chao (National Sun Yat-sen University, Taiwan), Yen-Che Yuan (National Sun Yat-sen University, Taiwan), Kun-Chih Chen (National Yang Ming Chiao Tung University, Taiwan)

09:24 am
ID1847: **High Reliable and Accurate Stochastic Computing-Based Artificial Neural Network Architecture Design**

Kun-Chih Chen (National Yang Ming Chiao Tung University, Taiwan), Wei-Ren Syu (National Sun Yat-sen University, Taiwan)

09:42 am
ID2489: Efficient Detection and Mitigation Schemes for Speculative Side Channels
Arash Pashrashid (National University of Singapore, Singapore), Ali Hajiabadi (National University of Singapore, Singapore), Trevor Carlson (National University of Singapore, Singapore)

8:30 am – 10:30 am
B1P-14 RF & Analog Amplifiers
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Vishal Saxena (University of Delaware)

ID1145: A Two-Stage CMOS Amplifier Performing High Degree of Stability for All Capacitive Load
Alessandro Bertolini (STMicroelectronics, Italy), Germano Nicollini (STMicroelectronics, Italy)

ID1771: Broadband High-Efficiency Continuous Class-F/F-1 Power Amplifiers with Active Second Harmonic Injection Technique
Chang Liu (Northwestern Polytechnical University, China), Yi Zhao (Northwestern Polytechnical University, China), Yue Yin (Northwestern Polytechnical University, China), He Guan (Northwestern Polytechnical University, China), Hao Zhang (Northwestern Polytechnical University, China), Fadhel Ghannouchi (University of Calgary, Canada)

ID1943: A Rail-to-Rail Input Class-AB Linear Amplifier with Improved Bandwidth and Slew-Rate for Envelope Tracking Supply Modulators
Surya Prasad Kondapalli (Indian Institute of Technology Kharagpur, India), Hemanth Pudi (Indian Institute of Technology Kharagpur, India), Debashis Mandal (Indian Institute of Technology Kharagpur, India)

ID2104: A 0.5-V Feedback-Based CMOS Buffer with Rail-to-Rail Operating Range
Feifan Gao (Nanyang Technological University, Singapore), Pak Kwong Chan (Nanyang Technological University, Singapore)

8:30 am – 10:30 am
B1P-15 Analog Signal Processing II
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Shahriar Mirabbasi (University of British Columbia)

ID1094: A BJT-Based Fully Integrated 16-Bit Zoom Temperature Sensor with an Inaccuracy of 0.28°C (3σ) from -40°C to 125°C Using Improved 1-Point Calibration
Xiaowei Zhang (Zhejiang University, China), Fuyue Qian (Zhejiang University, China), Jianxiong Xi (Zhejiang University, China), Lenian He (Zhejiang University, China)

ID1270: Design of Magnetic Field Acquisition Probe and Front-End Signal Processing Circuit
Guoqiang Li (Nanyang Technological University, Singapore), Yongfang Liu (Chinese Academy of Sciences, China), Yuanjin Zheng (Nanyang Technological University, Singapore)

ID1610: A Low-Power and High-Precision Time-Domain Winner-Take-All Circuit Based on the Group Search Algorithm
Hossein Yaghoobzadeh Shadmehri (Ferdowsi University of Mashhad, Iran), Ehsan Rahiminejad (Quchan University of Technology, Iran), Mehdi Saberi (École Polytechnique Fédérale de Lausanne, Switzerland), Alexandre Schmid (École Polytechnique Fédérale de Lausanne, Switzerland)

ID1746: Time-Encoded Mostly Digital Feature Extraction for Voice Activity Detection Tasks
Yukai Shen (Universidad Carlos III de Madrid, Spain), Carlos Perez (Infineon Technologies Austria, Austria), Dietmar Straeussnigg (Infineon Technologies Austria, Austria), Eric Gutierrez (Universidad Carlos III de Madrid, Austria)

8:30 am – 10:30 am
B1P-16 Low Power Logic, Circuits & Architectures III
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Mohsin Jamali (University of Texas Permian Basin)

ID1636: LWECC: A Lightweight ECC Technology for HPC Accelerators Supporting Multi-Granularity Memory Access
Lanting Guo (National University of Defense Technology, China), Haiyan Chen (National University of Defense Technology, China), Chen Li (National University of Defense Technology, China), Sheng Liu (National University of Defense Technology, China)

ID1677: High-Speed Phase-Based Computing
Nicholas Sica (Drexel University, United States), Ragh Kuttappa (Intel Corporation, United States), Vinayak Honkote (Intel Corporation, United States), Baris Taskin (Drexel University, United States)

ID1760: Design and Implementation of FPGA Based System for Object Detection and Range Estimation Used in ADAS Applications Utilizing FMCW Radar
Mujeev Khan (Aligarh Muslim University, India), Pranjal Mahajan (International Institute of Information Technology Hyderabad, India), Gani Nawaz Khan (Aligarh Muslim University, India), Devansh Chaudhary (Aligarh Muslim University, India), Jewel Benny (International Institute of Information Technology Hyderabad, India), Mohd Wajid (Aligarh Muslim University, India), Abhishek Srivastava (International Institute of Information Technology Hyderabad, India)

ID2021: Design and Analysis of an Energy-Efficient Duo-Core SRAM-Based Compute-in-Memory Accelerator
Lih-Yih Chiou (National Cheng Kung University, Taiwan), Hong-Ming Shih (National Cheng Kung University, Taiwan), Shun-Hsiu Hsu (National Cheng Kung University, Taiwan), Zu-Cheng Sheng (National Cheng Kung University, Taiwan), Soon-Jyh Chang (National Cheng Kung University, Taiwan)

8:30 am – 10:30 am
B1P-17 Low Power Logic, Circuits & Architectures IV
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Martinez Alonso Abdel (Tokyo Institute of Technology)

ID1097: DL-Sort: A Hybrid Approach to Scalable Hardware-Accelerated Fully-Streaming Sorting (TCAS-II paper)

Hyun Woo Oh (Seoul National University of Science and Technology, Korea), Joungmin Park (Seoul National University of Science and Technology, Korea), Seung Eun Lee (Seoul National University of Science and Technology, Korea)

ID1101: The Design of a Low-Latency Tensor Decomposition Algorithm and VLSI Architecture
Yu-An Chen (National Taiwan University of Science and Technology, Taiwan), Chung-An Shen (National Taiwan University of Science and Technology, Taiwan)

ID1852: A PCA Acceleration Algorithm for WiFi Sensing and its Hardware Implementation
He Wang (East China Normal University, China), Qitong Wang (East China Normal University, China), Leilei Huang (East China Normal University, China), Chunqi Shi (East China Normal University, China), Runxi Zhang (East China Normal University, China)

ID2025: A 15-Gb/s, 0.036 pJ/Bit, Half-Rate, Low Power PRBS Generator in 1.2 V, 65 nm CMOS
Ravibabu Perakalapudi (University of Hyderbad, India), Prema Kumar Govindaswamy (Indian Institute of Technology Bhubaneswar, India), Vijay Shankar Pasupureddi (Indian Institute of Technology Bhubaneswar, India)

ID2302: A 2.793µW Near-Threshold Neuronal Population Dynamics Simulator for Reliable Simultaneous Localization and Mapping
Zhengzhe Wei (Nanyang Technological University, Singapore), Boyi Dong (Nanyang Technological University, Singapore), Yuqi Su (Nanyang Technological University, Singapore), Yi Wang (Continental Automotive Singapore Pte. Ltd, Singapore), Chuanshi Yang (Virtus IC Design Center of Excellence, Nanyang Technological University, Singapore), Yuncheng Lu (Nanyang Technological University, Singapore), Chao Wang (Huazhong University of Science and Technology, China), Tony Tae-Hyoung Kim (Nanyang Technological University, Singapore), Yuanjin Zheng (Nanyang Technological University, Singapore)

8:30 am – 10:30 am
B1P-18 Circuits & Systems for Wireless Power Transfer
TRACK 4: POWER AND ENERGY CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Xi Chen (State Grid US Representative Office)

ID1130: An Efficiency-Enhanced Active Rectifier with Offset-Controlled Comparators for WPT Systems
Yuxuan Jiang (Imperial College London, United Kingdom), Zhiqiang Xu (Imperial College London, United Kingdom), Esther Rodriguez-Villegas (Imperial College London, United Kingdom)

ID1573: A Self-Powered P-SSHI Active Rectifier with Energy-Efficient Adaptive Switch Control for Piezoelectric Energy Harvesting
Yanjie Pan (Tianjin University, China), Simeng Yin (Tianjin University, China), Xiaguang Li (Tianjin University, China), Yixin Zhou (Southeast University, China), Keping Wang (Tianjin University, China)

ID1877: Time Domain Analysis of Secondary Stage with Series Resonance Driving Rectifier Load
Wing-Hung Ki (Hong Kong University of Science and Technology, Hong Kong), Yuan Yao (Hong Kong University of Science and Technology, Hong Kong), Chi-Ying Tsui (Hong Kong University of Science and Technology, Hong Kong)

ID1942: A Single-Stage Four-Phase Dual-Output Regulating Rectifier with Ultrafast Transient Response Using Double-Frequency Current-Wave Modulation
Weiyan Li (Fudan University, China), Xianren Hao (Beijing Smart-Chip Microelectronics Technology Co. Ltd., China), Xiaguang Li (Fudan University, China), Yan Ma (Beijing Smart-Chip Microelectronics Technology Co. Ltd., China), Jingjing Liu (Shanghai University, China), Huaxi Zhang (Tsinghua University, China), Xiaoyang Zeng (Fudan University, China), Zhiyuan Chen (Fudan University, China)

8:30 am – 10:30 am
B1P-19 Quantum Computing Circuits & Systems II
TRACK 5: BEYOND CMOS: NANOELECTRONICS AND HYBRID SYSTEMS INTEGRATION

Venue: Leo 2+3+4
POSTER
Session Chair(s): Vasileios Ntinas (TU Dresden)

ID1227: Energy-Efficient Ising Machines Using Capacitance-Coupled Latches for MaxCut Solving
Yimin Wang (National University of Singapore, Singapore), Xuanyao Fong (National University of Singapore, Singapore)

ID1761: Side-Channel Attacks Targeting Classical-Quantum Interface in Quantum Computers
Yerzhan Mustafa (University of Rochester, United States), Selcuk Köse (University of Rochester, United States)

ID2155: Boosting the Efficiency of Quantum Divider Through Effective Design Space Exploration
Siyi Wang (Nanyang Technological University, Singapore), Eugene Lim (Nanyang Technological University, Singapore), Anupam Chattopadhyay (Nanyang Technological University, Singapore)

ID2353: In-Memory Machine Learning Using Adaptive Multivariate Decision Trees and Memristors
Akash Chavan (Oakland University, United States), Pranav Sinha (Oakland University, United States), Sunny Raj (Oakland University, United States)

ID2439: Spatio-Temporal Characterization of Qubit Routing in Connectivity-Constrained Quantum Processors
Sahar Ben Rached (Universitat Politècnica de Catalunya, Spain), Carmen Garcia Almudéver (Universitat Politècnica de València, Spain), Eduard Alarcón (Universitat Politècnica de Catalunya, Spain), Sergi Abadal (Universitat Politècnica de Catalunya, Spain)

ID2285: Proposal & Investigation of Schottky Ring Engineered Reconfigurable Nanowire Transistor
Sourabh Panwar (Sardar Vallabhbhai National Institute of Technology, India), Shobhit Srivastava (Sardar Vallabhbhai National Institute of Technology, India), Shashidhara M (Sardar Vallabhbhai National Institute of Technology & People's Education Society University, India), Nithin Chatterji (Sardar Vallabhbhai National Institute of Technology, India), Prabhat Dubey (Università di Pisa, Italy), Deepak Joshi (Sardar Vallabhbhai National Institute of Technology, India), Abhishek Acharya (Sardar Vallabhbhai National Institute of Technology, India)

8:30 am – 10:30 am
B1P-20 Wearable Biomedical Circuits & Systems II

TRACK 6: BIOMEDICAL CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Pau-Choo Chung (National Cheng Kung University, Taiwan)

ID1625: High-Accuracy Stress Detection Using Wrist-Worn PPG Sensors
Anice Jahanjoo (Technische Universität Wien, Austria), Nima TaheriNejad (Heidelberg University, Germany), Amin Aminifar (Heidelberg University, Germany)

ID1751: Feature Points Based Residual UNet with Nonlinear Decay Rate for Partial Wet Fingerprint Restoration and Recognition
An-Ting Hsieh (National Tsing Hua University, Taiwan), Ching-Te Chiu (National Tsing Hua University, Taiwan), Tsai-Chieh Chen (National Tsing Hua University, Taiwan), Mao-Hsiu Hsu (National Formosa University, Taiwan), Wenyong Long (FocalTech Systems Co., Ltd., China)

ID2151: Flexible Integrated Circuits via Stress-Minimized Layout and Ultra-Thin Chip
Muyao Wang (Laboratory of Flexible Electronics Technology, Tsinghua University, China), Bo Wang (Zhejiang Tsinghua Institute of Flexible Electronics Technology, China), Lu Jia (Laboratory of Flexible Electronics Technology, Tsinghua University, China), Haicheng Li (Laboratory of Flexible Electronics Technology, Tsinghua University, China), Xue Feng (Laboratory of Flexible Electronics Technology, Tsinghua University, China)

8:30 am – 10:30 am
B1P-21 Neural Learning Systems: Optimizations & Applications II
TRACK 8: NEURAL NETWORKS AND NEUROMORPHIC ENGINEERING

Venue: Leo 2+3+4
POSTER
Session Chair(s): Yang Zhao (Shanghai Jiaotong University)

ID1375: Streamlining DNN Obfuscation to Defend Against Model Stealing Attacks
Yidan Sun (Nanyang Technological University, Singapore), Siew-Kei Lam (Nanyang Technological University, Singapore), Guiyuan Jiang (Ocean University of China, China), Peilan He (Ocean University of China, China)

ID1974: Data-Free Learning for Lightweight Multi-Weather Image Restoration
Pei Wang (Xiamen University, China), Hongzhan Huang (Xiamen University, China), Xiaotong Luo (Xiamen University, China), Yanyun Qu (Xiamen University, China)

ID2164: FPGA Implementation for Large Scale Reservoir Computing Based on Chaotic Boltzmann Machine
Shigeki Matsumoto (IVIS, Inc., Japan), Yuki Ichikawa (IVIS, Inc., Japan), Nobuki Kajihara (IVIS, Inc., Japan), Hakaru Tamukoh (Kyushu Institute of Technology, Japan)

ID1295: Amalgamating Knowledge for Comprehensive Classification with Uncertainty Suppression
Lebin Li (Southwest University of Science and Technology, China), Ning Jiang (Southwest University of Science and Technology, China), Jialiang Tang (Nanjing University of Science and Technology, China), Xinlei Huang (Southwest University of Science and Technology, China)

ID1381: A Highly Reliable PPG Authentication System Based on an Improved AI Model with Dynamic Weighted Triplet Loss Function
Yang Yang (National Yang Ming Chiao Tung University, Taiwan), Wai-Chi Fang (National Yang Ming Chiao Tung University, Taiwan)

ID1756: [Efficient Neural Compression with Inference-Time Decoding]
Clement Metz (Université Paris-Saclay, CEA List, France), Olivier Bichler (Université Grenoble Alpes, CEA List, France), Antoine Dupret (Université Grenoble Alpes, CEA-Leti, France)

ID1200: [Empirical Study on the Impact of Few-Cost Proxies]
Kevin Kollek (University of Wuppertal, Germany), Marco Braun (University of Wuppertal, Germany), Jan-Hendrik Meusener (University of Wuppertal, Germany), Jan-Christoph Krabbe (University of Wuppertal, Germany), Anton Kummert (University of Wuppertal, Germany)

8:30 am – 10:30 am
B1P-22 Compressive Sensing & Sparsity Applications
TRACK 10: DIGITAL SIGNAL PROCESSING

Venue: Leo 2+3+4
POSTER
Session Chair(s): Mrityunjoy Chakrabor (Indian Institute of Technology (IIT), Kharagpur)

ID1475: [Two-Stage Adaptive Compressive Sensing and Reconstruction for Terahertz Single-Pixel Imaging]
Yu-Kai Zhang (National Tsing Hua University, Taiwan), Che-Yu Chou (National Tsing Hua University, Taiwan), Shang-Hua Yang (National Tsing Hua University, Taiwan), Yuan-Hao Huang (National Tsing Hua University, Taiwan)

ID1743: [Hard Thresholding Based Stochastic Robust Algorithm for Multiple Measurement Vectors]
Ketan Atul Bapat (Indian Institute of Technology Kharagpur, India), Shashank S (Indian Institute of Technology Kharagpur, India), Mrityunjoy Chakraborty (Indian Institute of Technology Kharagpur, India)

ID2062: [Interpolation and Extrapolation by Prolate Spheroidal Wave Functions Using Nonuniform Division and Generalized Chirp Modulation]
Chun-Jen Shih (National Taiwan University, Taiwan), Jian-Jiun Ding (National Taiwan University, Taiwan)

ID2289: [Wideband DOA Estimation Based on Tensor Completion and Decomposition]
Kangning Li (Beijing Institute of Technology, China), Qing Shen (Beijing Institute of Technology, China), Wei Liu (Queen Mary University of London, United Kingdom), Min Wang (Beijing Institute of Technology, China)

ID2351: [Acquisition and Processing of Chromatic Derivatives Using FPGA-Based Digital Hardware]
Zhaofeng Zhong (University of Queensland, Australia), Pathmapirian Nanthakumar (University of Queensland, Australia), Gabriel Field (University of Queensland, Australia), Chamira U. S. Edussooriya (University of Moratuwa, Sri Lanka), Aleksandar Ignjatovic (University of New South Wales, Australia), Chamith Wijenayake (University of Queensland, Australia)

8:30 am – 10:30 am
B1P-23 Applications of Non-Linear Circuits & Systems
TRACK 9: METHODS AND MODELS FOR THE ANALYSIS/DESIGN OF NONLINEAR CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER

Session Chair(s): Michael Peter Kennedy (University College Dublin), Giuseppe Grassi (University of Salento, Italy)

ID1004: **A Two-Step Fine-Tuning Assisted Layout Sizing Scheme for Analog/RF Circuits**
Zhikai Wang (Tsinghua University, China), Zuochang Ye (Tsinghua University, China), Jingbo Zhou (Baidu Research, China), Xiaosen Liu (Tsinghua University, China), Yan Wang (Tsinghua University, China)

ID1077: **Fast Simulation of Circuits with Recursive Elements: Application to a BESS**
Federico Bizzarri (Politecnico di Milano, Italy), Angelo Maurizio Brambilla (Politecnico di Milano, Italy), Davide Del Giudice (Politecnico di Milano, Italy), Daniele Linaro (Politecnico di Milano, Italy)

ID1559: **New Measure for Network Controllability Robustness Based on Controllable Subspace**
Yan Wen Liu (Fudan University, China), Jie Ding (Fudan University, China), Xiang Li (Fudan University & Tongji University, China)

ID1627: **Characterization and Mitigation of ADC Noise by Reference Tuning in RRAM-Based Compute-in-Memory**
Ying-Hao Wei (Georgia Institute of Technology, United States), Zishen Wan (Georgia Institute of Technology, United States), Brian Crafton (Georgia Institute of Technology, United States), Samuel Spetalnick (Georgia Institute of Technology, United States), Arijit Raychowdhury (Georgia Institute of Technology, United States)

ID2211: **Battery Modeling with Mittag-Leffler Function**
Shahinda Abdelhafiz (Nile University, Egypt), Mohammed Fouda (Rain Neuromorphics Inc., United States), Ahmed Radwan (Nile University, Egypt)

ID1107: **Analysis of Current-Commutating Passive and Active Mixers for mmWave Applications**
Kimi Jokiniemi (Aalto University, Finland), Kaisa Ryynänen (Aalto University, Finland), Joni Vähä (Aalto University, Finland), Kari Stadius (Aalto University, Finland), Jussi Ryynänen (Aalto University, Finland)

8:30 am – 10:30 am
B1P-24 Artificial Intelligence in Power & Energy Circuits & Systems II
TRACK 14: SPECIAL SESSION

Venue: Leo 2+3+4
POSTER
Session Chair(s): Herbert Ho-Ching Lu (University of Western Australia), Junrui Liang (ShanghaiTech University)

ID2138: **Modeling of DC-DC Converters with Neural Ordinary Differential Equations**
Hanchen Ge (South China University of Technology, China), Canjun Yuan (South China University of Technology, China), Yaofeng Liang (South China University of Technology, China), Jinpeng Lei (South China University of Technology, China), Zhicong Huang (South China University of Technology, China)

ID2315: **Power System Events Classification Technology Based on Deep-Learning**
Xin Lei (Beijing Institute of Technology, China), Hongwei Ma (Beijing Institute of Technology, China), Bin Liu (China University of Petroleum, China), Zhen Li (Beijing Institute of Technology, China)

8:30 am – 10:30 am
B1P-25 Theory & Applications of Memristor Devices, Circuits, & Systems for Bio-Inspired Electronics II
TRACK 14: SPECIAL SESSION

Venue: Leo 2+3+4
POSTER
Session Chair(s): Alon Ascoli (Technische Universität Dresden), Alex James (Digital University Kerala)

ID1596: Smart Clothing Using Antenna and Memristive ANN
Elizabeth George (Digital University Kerala, India), Sruthi Pallathuvalappil (Digital University Kerala, India), Alex James (Digital University Kerala, India)

ID1748: Realization of Reading-Based Ternary Łukasiewicz Logic Using Memristive Devices
Feng Liu (Forschungszentrum Jülich GmbH, Germany), Xianyue Zhao (Friedrich Schiller University Jena, Germany), Ziang Chen (Friedrich Schiller University Jena, Germany), Christopher Bengel (RWTH Aachen University, Germany), Nan Du (Friedrich Schiller University Jena, Germany), Stephan Menzel (Forschungszentrum Jülich GmbH, Germany)

ID2012: High Voltage Transformer Condition Monitoring Using Memristive Echo State Networks
Vineeta Vasudevan Nair (Digital University Kerala, India), Anilkumar P (Digital University Kerala, India), Alex James (Digital University Kerala, India)

10:00 am – 10:30 am
Coffee Break
NETWORKING

10:30 am – 11:30 am
Semiconductor Innovations to Continue and Go Beyond Moore's Law in the Era of AI
KEYNOTE

Venue: B2 Ballroom
Speaker: Hemanth Jagannathan, Distinguished Engineer, Chiplet and Advanced Packaging Technology,
IBM Research, USA
Session Chair(s): Rajiv Joshi (IBM, USA)

11:30 am – 12:30 pm
The Evolving Power Grid Towards a Greener Future
KEYNOTE

Venue: B2 Ballroom
Speaker: Michael Tse, Chair Professor of Electrical Engineering and Associate Vice President, City University of Hong Kong, Hong Kong
Session Chair(s): Yoshifumi Nishio (Tokushima University, Japan)

12:30 pm – 1:30 pm
Lunch
NETWORKING

Venue: B2 Ballroom

1:30 pm – 2:00 pm
Award Ceremony
SPECIAL EVENT

Venue: Leo 1
Session Chair(s): Myung Hoon Sunwoo (Ajou University, South Korea), Manuel Delgado-Restituto (Microelectronics Institute of Sevilla, Spain)

2:00 pm – 2:30 pm
CASS 75th Anniversary
SPECIAL EVENT

Venue: B2 Ballroom
Session Chair(s): Yongfu Li (Shanghai Jiao Tong University, China), Fakhrul Zaman Rokhani (Universiti Putra Malaysia, Malaysia), Myung Hoon Sunwoo (Ajou University, Korea)

2:30 pm – 3:30 pm
Past President Sharing Panel
SPECIAL EVENT

Venue: B2 Ballroom
Panellists: Franco Maloberti (University of Parma), Sung Mo (Steve) Kang (University of California), and Ljiljana Trajkovic (Simon Fraser University)
Session Chair(s): Amara Amara (Beihang University, China), Yongfu Li (Shanghai Jiao Tong University, China), Yoko Uwate (Tokushima University)

3:30 pm – 4:00 pm
Coffee Break
NETWORKING

3:30 pm – 5:30 pm
B4P-14 Pipelined & Time Interleaved ADC
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Xinsheng Wang (Harbin Institute of Technology)

ID1050: A DAC Sharing and Linearization Technique for Time-Interleaved Incremental Delta-Sigma ADCs
Jesko Flemming (Hochschule Hannover - University of Applied Sciences and Arts, Germany), Bernhard Wicht (Leibniz University Hannover, Germany), Pascal Witte (Hochschule Hannover - University of Applied Sciences and Arts, Germany)

ID1099: Hardware-Implemented Calibration Based on Sinusoidal Fitting for Hybrid Pipeline ADC
Yuguo Xiang (Fudan University, China), Yutong Zhao (Fudan University, China), Dayan Zhou (Fudan University, China), Danfeng Zhai (Fudan University, China), Junyan Ren (Fudan University, China), Fan Ye (Fudan University, China)

ID1558: A Reconfigurable Continuous-Time Delta-Sigma Modulator Structure Using Hybrid Loop Filter and Time-Interleaved Quantizer

Chen Chen (Tsinghua University, China), Fangzhen Jiang (Tsinghua University, China), Peng Wang (Tsinghua University, China), Yongli Chen (Beijing Smart-Chip Microelectronics Technology Co. Ltd., China), Yan Xiao (Beijing Smart-Chip Microelectronics Technology Co. Ltd., China), Fule Li (Tsinghua University, China), Xiang Xie (Tsinghua University, China)

ID2098: **A Low Power 16-Bit 125MS/s Pipeline ADC with 100dB SFDR**
Xiaodan Zhou (University of Electronic Science and Technology of China, China), Weipeng He (University of Electronic Science and Technology of China, China), Chen Su (GigaChip Technology Co. Ltd, China), Tao Liu (GigaChip Technology Co. Ltd, China), Dongbing Fu (GigaChip Technology Co. Ltd, China), Qiang Li (University of Electronic Science and Technology of China, China)

ID2441: **Utilization of Noise-Shaping in Mixed-Signal Timing-Skew Mismatch Calibration of TI-ADCs**
Hamidreza Mafi (Polytechnique Montréal, Canada), Mohamed-Amine Bensenouci (Polytechnique Montréal, Canada), Sadok Aouini (Ciena Corporation, Canada), Mohammad Honarparvar (Ciena Corporation, Canada), Naim Ben-Hamida (Ciena Corporation, Canada), Yvon Savaria (Polytechnique Montréal, Canada)

3:30 pm – 5:30 pm
B4P-15 Analog & Mixed Signal Circuits & Systems
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Filippo Neri (Renesas Electronics, Zürich, Switzerland)

ID1386: **A V-Band Low-Phase-Noise VCO with Transformer-Based Gm-Boosting Technique**
Biao Wang (Sun Yat-sen University, China), Xiangyu Meng (Sun Yat-sen University, China), Fangfei Ming (Sun Yat-sen University, China)

ID1633: **A Trimming-Less External-RC Relaxation Oscillator with Self-Calibrating Current Reference for a SiC Active Gate Driver Application**
Erik Wehr (RWTH Aachen University, Germany), Tobias Zekorn (RWTH Aachen University, Germany), Michael Hanhart (RWTH Aachen University, Germany), Kenny Vohl (RWTH Aachen University, Germany), Leon Weihs (Integrated Analog Circuits and RF Systems, RWTH Aachen University, Germany), Ralf Wunderlich (RWTH Aachen University, Germany), Stefan Heinen (RWTH Aachen University, Germany)

ID1882: **A Differential SPDT T/R Switch for PMUT Biomedical Ultrasound Systems**
Yaohua Zhang (University College London, United Kingdom), Dai Jiang (University College London, United Kingdom), Andreas Demosthenous (University College London, United Kingdom)

ID2051: **Toward Accurate Analysis of Channel Charge Injection in SAR ADCs' Capacitive DACs**
Alireza Ahrar (York University, Canada), Jianxong Xu (University of Toronto, Canada), Mohammad Reza Pazhouhandeh (University of Toronto, Canada), Antoine Frappe (York University, Canada), Mostafa Rahimi Azghadi (James Cook University, Australia), Amirali Amirsoleimani (York University, Canada)

ID2407: **A 136μW Over 800M Range Backscatter-Like UHF Band Transceiver**
Ling Hao (Peking University, China), Keer Gao (Peking University, China), Haoyu Bai (Peking University, China), Chuancheng Wu (Peking University, China), Dong Wang (Peking University,

China), Sihao Zhang (Peking University, China), Jiazheng Zhou (Peking University, China), Junhua Liu (Peking University, China), Huailin Liao (Peking University, China)

ID1569: **A 70dB SNDR 20MHz-BW VCO-Based CT Sturdy MASH Delta-Sigma Modulator with Robust Quantization Error Extraction**
Xinpeng Gui (Tsinghua University, China), Xinfa Zheng (Katholieke Universiteit Leuven, Belgium), Haigang Feng (Tsinghua University, China), Georges Gielen (Katholieke Universiteit Leuven, Belgium), Zhihua Wang (Tsinghua University, China), Xinpeng Xing (Sun Yat-sen University, China)
ID1814: Current-Steering DAC Architecture Design for Amplitude Mismatch Error Minimization
Ramin Babaee (University of Ottawa, Canada), Shahab Oveis Gharan (Ciena Corporation, Canada), Martin Bouchard (University of Ottawa, Canada)

ID1686: **A Mixed-Signal TIA with Input Restoring ADC**
David-Peter Wiens (Universität Ulm, Germany), Björn Driemeyer (Universität Ulm, Germany), Maurits Ortmanns (Universität Ulm, Germany)

ID2343: **Pseudo-Differential Time-to-Amplitude Converter for LGAD Based Particle Detectors**
Simone Giroletti (University of Pavia & INFN Pavia, Italy), Lodovico Ratti (University of Pavia & INFN Pavia, Italy), Carla Vacchi (University of Pavia & INFN Pavia, Italy)

ID2035: **Edge-Weighted Graph Neural Networks for Post-Placement Interconnect Capacitance Estimation of Analog Circuits**
Zhengfeng Wu (Drexel University, United States), Ioannis Savidis (Drexel University, United States)

3:30 pm – 5:30 pm
B4P-16 Digital Circuits, Systems & Architecture for Machine Learning VII
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Robert Chen-Hao Chang (University of Western Ontario)

ID1708: **ALPACA: An Accelerator Chip for Nested Loop Programs**
Dominik Walter (Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany), Marcel Brand (Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany), Christian Heidorn (Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany), Michael Witterauf (Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany), Frank Hannig (Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany), Jürgen Teich (Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany)

ID2007: **Adversarial Label Flipping Attack on Supervised Machine Learning-Based HT Detection Systems**
Richa Sharma (Bennett University, Times Group, India), G.K. Sharma (Atal Bihari Vajpayee Indian Institute of Information Technology and Management, India), Manisha Pattanaik (Atal Bihari Vajpayee Indian Institute of Information Technology and Management, India)

ID1208: **A Hardware-Friendly Alternative to Softmax Function and its Efficient VLSI Implementation for Deep Learning Applications**
Meng-Hsun Hsieh (National Yang Ming Chiao Tung University, Taiwan), Xuan-Hong Li (National Yang Ming Chiao Tung University, Taiwan), Yu-Hsiang Huang (National Yang Ming Chiao Tung University, Taiwan), Pei-Hsuan Kuo (National Yang Ming Chiao Tung University, Taiwan), Juinn-Dar Huang (National Yang Ming Chiao Tung University, Taiwan)

ID1839: **Neural Network Acceleration Using Digit-Plane Computation with Early Termination**

Shen-Fu Hsiao (National Sun Yat-sen University, Taiwan), Hou-Chun Kuo (National Sun Yat-sen University, Taiwan), Yu Kuo (National Sun Yat-sen University, Taiwan), Kun-Chih Chen (National Yang Ming Chiao Tung University, Taiwan)

ID2517: POCO: Hardware Characterization of Activation Functions Using POSIT-CORDIC Architecture
Mahati Basavaraju (International Institute of Information Technology Bangalore, India), Vinay Rayapati (International Institute of Information Technology Bangalore, India), Madhav Rao (International Institute of Information Technology Bangalore, India)

3:30 pm – 5:30 pm
B4P-17 Advanced Techniques for Digital Integrated Circuits & Systems II
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Mircea Stan (University of Virginia)

ID1032: Unified-Pipelined NTT Architecture for Polynomial Multiplication in Lattice-Based Cryptosystems
Trong-Hung Nguyen (University of Electro-Communications, Japan), Nguyen The Binh (Ho Chi Minh City University of Technology, Vietnam), Huynh Phuc Nghi (Ho Chi Minh City University of Technology, Vietnam), Cong-Kha Pham (University of Electro-Communications, Japan), Trong-Thuc Hoang (University of Electro-Communications, Japan)

ID1157: Optimization of TDM Using Single-Ended Transmission for Multi-FPGA Platforms
Haoyu Liao (National University of Defense Technology, China), Yuan Li (National University of Defense Technology, China), Puguang Liu (National University of Defense Technology, China), Qiang Wang (National University of Defense Technology, China), Mingche Lai (National University of Defense Technology, China), Xingyun Qi (National University of Defense Technology, China)

ID1931: An Efficient FPGA Implementation of a Simple Lossless Algorithm (SLA) for On-Board Satellite Hyperspectral Data Compression
Vijay Joshi (Indian Institute of Space Science and Technology, India), Sheeba Rani J. (Indian Institute of Space Science and Technology, India)

ID2370: RISCALAR: A Cycle-Approximate, Parametrisable RISC-V Microarchitecture Explorer & Simulator
Josiah Mendes (Imperial College London, United Kingdom), Rajesh Panicker (National University of Singapore, Singapore)

ID2410: A Timing-Shared Adaptive Sensing Methodology for Low-Voltage SRAM
Yongliang Zhou (Anhui University, China), Zhen Yang (Anhui University, China), Yiming Wei (Anhui University, China), Xiao Lin (Anhui University, China), Saiai Wu (Anhui University, China), Wenjuan Lu (Anhui University, China), Chunyu Peng (Anhui University, China), Xin Li (Anhui University, China), Xiulong Wu (Anhui University, China)

3:30 pm – 5:30 pm
B4P-18 Power Converters & Charge Pumps
TRACK 4: POWER AND ENERGY CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Mo Huang (University of Macau)

ID1248: A Fully Integrated Charge Pump with Double-Loop Control and Differentiator-Based Transient Enhancer for Neural Stimulation Applications
Liwei Cao (Fudan University, China), Xiao Liu (Fudan University, China)

ID1578: A 5V-Input Sub-1V-Output Single-Inductor Multi-Path Hybrid Buck Converter Achieving 96.1% Peak Efficiency with 250mΩ DCR Inductor
Jiebao Li (Guangzhou University, China), Yongfu Li (Shanghai Jiao Tong University, China), Yanhan Zeng (Guangzhou University, China)

ID1644: Design Considerations for DC-DC Voltage Regulators in Distributed Vertical Power Delivery Systems
Sriharini Krishnakumar (University of Illinois, Chicago, United States), Mingeun Choi (Georgia Institute of Technology, United States), Ramin Rahimzadeh Khorasani (Pennsylvania State University, United States), Rohit Sharma (Indian Institute of Technology Ropar, India), Madhavan Swaminathan (Pennsylvania State University, United States), Satish Kumar (Georgia Institute of Technology, United States), Inna Partin-Vaisband (University of Illinois, Chicago, United States)

ID1557: A 12V-to-1~1.8V Tri-Path Series-Capacitor Converter with Reduced Inductor Current and Full-Range Duty Cycle for Point-of-Loads Application
Haoxin Cai (South China University of Technology, China), Bin Li (South China University of Technology, China), Zhaohui Wu (South China University of Technology, China)

3:30 pm – 5:30 pm
B4P-19 Wireline & Optical Communications
TRACK 3: COMMUNICATIONS CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Wael Badawy (the International Centre for Arbitration, Egypt), Jongsun Park (Korea University)

ID1983: DMT 3L4W: A 3-Lane 4-Wire Signaling with Discrete Multitone Modulation for High-Speed Wireline Chip-to-Chip Interconnects
Seoyoung Jang (Daegu Gyeongbuk Institute of Science and Technology, Korea), Jaewon Lee (Daegu Gyeongbuk Institute of Science and Technology, Korea), Yujin Choi (Daegu Gyeongbuk Institute of Science and Technology, Korea), Donggeon Kim (Daegu Gyeongbuk Institute of Science and Technology, Korea), Gain Kim (Daegu Gyeongbuk Institute of Science and Technology, Korea)

ID2158: A Novel Channel-Aware, Non-Sampling UART Receiver with Augmented Clock Frequency Resilience (TCAS-II paper)
Timothy Simon Thomas (PI Semiconductor (Shenzhen) Co.,Ltd., India), Arun Singh (PI Semiconductor (Shenzhen) Co.,Ltd., India), Shyam Ramanathan (PI Semiconductor (Shenzhen) Co.,Ltd., India), Sunil Rafeeque (PI Semiconductor (Shenzhen) Co.,Ltd., India)

ID2294: A Semi-Folded Based High-Power-Efficiency FFT for Frequency Offset Estimate
Liyu Lin (Fudan University, China), Jingguo Wu (Fudan University, China), Xiaoyang Zeng (Fudan University, China), Yun Chen (Fudan University, China)

ID2352: Interleaving Active Feedback in Inverter-Based Optical Receivers for Bandwidth Extension and Linearity Improvement
Sara Radfar (Concordia University, Canada), Glenn Cowan (Concordia University, Canada)

3:30 pm – 5:30 pm
B4P-20 Biomedical Signal/Image Processing, Circuits & Systems
TRACK 6: BIOMEDICAL CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Yu Wu (University College London, UK)

ID1496: Design and FPGA Implementation of a Light-Weight Calibration-Friendly Eye Gaze Tracking Algorithm
Tianyi Liu (Tsinghua University, China), Xuecheng Wang (Tsinghua University, China), Guolin Li (Tsinghua University, China), Milin Zhang (Tsinghua University, China)

ID1505: FPGA Based Adaptive Receive Apodization Design for Diagnostic Ultrasound Imaging
Gayathri Malamal (Indian Institute of Technology Palakkad, India), Mahesh Raveendranatha Panicker (Singapore Institute of Technology, Singapore)

ID1940: Advancing In-Home Gait Monitoring: A Feasibility Study of Upper Limb Swing Analysis Using FMCW Radar
Easha Easha (Indian Institute of Science, India), Gaurab Banerjee (Indian Institute of Science, India)

ID2053: An FPGA-Based, Multi-Channel, Real-Time, Motion Artifact Detection Technique for fNIRS/DOT Systems
Yunjia Xia (University College London, United Kingdom), Elisabetta Maria Frijia (University College London, United Kingdom), Rui Loureiro (University College London, United Kingdom), Robert J. Cooper (University College London, United Kingdom), Hubin Zhao (University College London, United Kingdom)

3:30 pm – 5:30 pm
B4P-21 Neuromorphic Systems III
TRACK 8: NEURAL NETWORKS AND NEUROMORPHIC ENGINEERING

Venue: Leo 2+3+4
POSTER
Session Chair(s): Fernando Perez Peña (Universidad de Cádiz)

ID1162: SSDC: A Scalable Sparse Differential Checkpoint for Large-Scale Deep Recommendation Models
Lingrui Xiang (Southern University of Science and Technology, China), Xiaofen Lu (Southern University of Science and Technology, China), Rui Zhang (RAMS Lab, Huawei, China), Zheng Hu (RAMS Lab, Huawei, China)

ID1770: A Charge-Trap-Transistor-Based Fully Analog Machine Learning Inference Engine for Audio Keyword Spotting
Navid Rezazadeh (Blumind, Canada), John Gosson (Blumind, Canada), Roger Levinson (Blumind, Canada), Paramjeet Sahni (Blumind, Canada), Mark Bury (Blumind, Canada), Juan Diaz (Blumind, Canada), Shufan Chan (Blumind, Canada), Eve Boyer (Blumind, Canada), Niraj Mathur (Blumind, Canada), Hamid Taheri (Blumind, Canada)

ID1892: Neuromorphic Energy Efficient Stress Detection System Using Spiking Neural Network
Ajay B S (Intel Technology India Pvt. Ltd., India), Madhav Rao (International Institute of Information Technology Bangalore, India), Phani Pavan Kambhampati (International Institute of Information Technology Bangalore, India)

ID2027: [Neural-Inspired Dendritic Multiplication Using a Reconfigurable Analog Integrated Circuit]
Jordan Edwards (Baylor University, United States), Luke Parker (Baylor University, United States), Suma Cardwell (Sandia National Laboratories, United States), Frances Chance (Sandia National Laboratories, United States), Scott Koziol (Baylor University, United States)

ID1721: [SPRCPI: An Efficient Tool for SNN Models Deployment on Multi-Core Neuromorphic Chips via Pilot Running]
Liangshun Wu (Shanghai Jiao Tong University, China), Lisheng Xie (Shanghai Jiao Tong University, China), Jianwei Xue (Shanghai Jiao Tong University, China), Faquan Chen (Shanghai Jiao Tong University, China), Qingyang Tian (Shanghai Jiao Tong University, China), Yifan Zhou (Shanghai Jiao Tong University, China), Ziren Wu (Shanghai Jiao Tong University, China), Rendong Ying (Shanghai Jiao Tong University, China), Peilin Liu (Shanghai Jiao Tong University, China)

ID1727: [An SRAM Compute-in-Memory Macro Based on Direct Coupling SAR ADC and DAC Reuse]
Yongteng Ma (Zhejiang University, China), Xuliang Yu (Zhejiang University, China), Zhichao Tan (Zhejiang University, China), Liang Zhao (Zhejiang University, China)

3:30 pm – 5:30 pm
B4P-22 Imaging & Sensing
TRACK 10: DIGITAL SIGNAL PROCESSING

Venue: Leo 2+3+4
POSTER
Session Chair(s): Tong Zhou (Nanjing University of Science and Technology)

ID1518: [A Field Deployable Imaging System for Detecting Microplastics in the Aquatic Environment]
Jianqing Huang (University of Hong Kong, Hong Kong), Yuxing Li (University of Hong Kong, Hong Kong), Yanmin Zhu (University of Hong Kong, United States), Edmund Lam (University of Hong Kong, Hong Kong)

ID2451: [LIRSRN: A Lightweight Infrared Image Super-Resolution Network]
Chun-An Lin (National Chung Hsing University, Taiwan), Tsung-Jung Liu (National Chung Hsing University, Taiwan), Kuan-Hsien Liu (National Taichung University of Science and Technology, Taiwan)

ID2470: [Improved Camera Calibration Method Using Complementary Patterns]
Xuguang Zhang (Tsinghua University, China), Jiawen Xue (Tsinghua University, China), Wei Song (Tsinghua University, China), Guolin Li (Tsinghua University, China), Xiang Xie (Tsinghua University, China)

ID2251: [A Multi-Scale Block PatchMatch-Based Unified Algorithm for Efficient 6-D Vision Processing]
Hongyu Wang (ShanghaiTech University, China), Xiangyu Zhang (ShanghaiTech University, China), Xin Lou (ShanghaiTech University, China)

ID1793: [FPSeg: Flexible Promptable Semantic Segmentation for Edge Devices]
Jan-Christoph Krabbe (University of Wuppertal, Germany), Adrian Bauer (University of Wuppertal, Germany), Kevin Kollek (University of Wuppertal, Germany), Jan-Hendrik Meusener (University of Wuppertal, Germany), Anton Kummert (University of Wuppertal, Germany)

ID 2613: CMOS/MEMS Integration Approaches for Miniaturized Sensors
Nooshin Saeidi (Fraunhofer Institute, Germany) and Virgilio Valente (Toronto Metropolitan University, Canada)

3:30 pm – 5:30 pm
B4P-23 Live Demo II
TRACK 15: LIVE DEMO

Venue: Leo 2+3+4
POSTER
Session Chair(s): Deruo Cheng (Nanyang Technological University), Chao Wang (Huazhong University of Science and Technology)

ID1164: Live Demonstration: Man-in-the-Middle Attack on Edge Artificial Intelligence
Bowen Hu (Nanyang Technological University, Singapore), Weiyang He (Nanyang Technological University, Singapore), Si Wang (Nanyang Technological University, Singapore), Wenye Liu (Nanyang Technological University, Singapore), Chip Hong Chang (Nanyang Technological University, Singapore)

ID1172: Live Demonstration: A Mixed-Mode Signal CMOS Chip for Hyperdimensional Computing
Daniel García-Lesta (Universidade de Santiago de Compostela, Spain), Fernando Pardo (Universidade de Santiago de Compostela, Spain), Oscar Pereira-Rial (Universidade de Santiago de Compostela, Spain), Victor Brea (Universidade de Santiago de Compostela, Spain), Paula López (Universidade de Santiago de Compostela, Spain), Diego Cabello (Universidade de Santiago de Compostela, Spain)

ID1277: Live Demonstration: Automated Design of Analog and Mixed-Signal Circuits Using Neural Networks
Gustavo Liñán-Cembrano (IMSE-CNM, CSIC & Universidad de Sevilla, Spain), Jose de la Rosa (IMSE-CNM, CSIC & Universidad de Sevilla, Spain)

ID1278: Live Demonstration: Using ANNs to Predict the Evolution of Spectrum Occupancy
Gustavo Liñán-Cembrano (IMSE-CNM, CSIC & Universidad de Sevilla, Spain), Jose de la Rosa (IMSE-CNM, CSIC & Universidad de Sevilla, Spain)

ID1605: Live Demonstration: A 5-DC-Parameter MOSFET Model for Circuit Design and Simulation Using Open-Source EDA Tools
Gabriel Maranhão (Federal University of Santa Catarina, Brazil), Deni Germano Alves Neto (Federal University of Santa Catarina, Brazil), Marcio Cherem Schneider (Federal University of Santa Catarina, Brazil), Carlos Galup-Montoro (Federal University of Santa Catarina, Brazil)

ID2293: Live Demonstration for Input-Sparsity-Aware RRAM Processing-in-Memory Chip
Junjie Wang (University of Electronic Science and Technology of China, China), Shuang Liu (University of Electronic Science and Technology of China, China), Ruicheng Pan (University of Electronic Science and Technology of China, China), Shiqin Yan (University of Electronic Science and Technology of China, China), Yihe Liu (University of Electronic Science and Technology of China, China), Yang Liu (University of Electronic Science and Technology of China, China)

3:30 pm – 5:30 pm
B4P-24 Education in Circuits & Systems II
TRACK 13: EDUCATION IN CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4

POSTER
Session Chair(s): Babak Ayazifar (University of California, Berkeley), Ljiljana Trajkovic (Simon Fraser University)

ID1109: A Challenge-Based Blended Learning Approach for an Introductory Digital Circuits and Systems Course
Julian Hoefer (Karlsruhe Institute of Technology, Germany), Michael Gauß (Karlsruhe Institute of Technology, Germany), Manuela Adams (Karlsruhe Institute of Technology, Germany), Fabian Kreß (Karlsruhe Institute of Technology, Germany), Fabian Kempf (Karlsruhe Institute of Technology, Germany), Christian Karle (Karlsruhe Institute of Technology, Germany), Tanja Harbaum (Karlsruhe Institute of Technology, Germany), Andreas Barth (Karlsruhe Institute of Technology, Germany), Jürgen Becker (Karlsruhe Institute of Technology, Germany)

ID2082: Curriculum Development for Tapeout-Ready Mixed-Signal System-on-Chip Design and Assembly
Samuel Murray (University of Nebraska–Lincoln, United States), Joseph Schmitz (University of Nebraska–Lincoln, United States), Sina Balkir (University of Nebraska--Lincoln, United States), Michael Hoffman (University of Nebraska--Lincoln, United States)

ID2114: Systematic Development of CMOS PTAT Circuits
Shanthi Pavan (Indian Institute of Technology Madras, India)

ID2361: Improving High School Math Engagement with Circuit and Transistor Examples
Andrew Ash (Oklahoma State University, United States), John Hu (Oklahoma State University, United States)

ID2368: Leveraging Open Source IC Design Tools for an Undergraduate Microelectronic Circuit Design Course
Astria Nur Irfansyah (Institut Teknologi Sepuluh Nopember, Indonesia)

3:30 pm – 5:30 pm
B4P-25 Optimization & Machine Learning for Signal Processing
TRACK 10: DIGITAL SIGNAL PROCESSING

Venue: Leo 2+3+4
POSTER
Session Chair(s): Mohsin Jamali (University of Texas Permian Basin)

ID1352: Adaptive Weighting Feature Aggregation Using Particle Swarm Optimization for Image Retrieval
Farzad Sabahi (Concordia University, Canada), M. Omair Ahmad (Concordia University, Canada), M.N.S. Swamy (Concordia University, Canada)

ID1650: A Precise and Reliable Engine Knock Detection Utilizing Meta Classifier
Amirhossein Moshrefi (École de Technologie Supérieure ÉTS, Canada), Yves Blaquière (École de Technologie Supérieure ÉTS, Canada), Frédéric Nabki (École de Technologie Supérieure ÉTS, Canada)

ID1691: Audio-Visual Cross-Modal Generation with Multimodal Variational Generative Model
Zhubin Xu (Hangzhou Dianzi University, China), Tianlei Wang (Hangzhou Dianzi University, China), Dekang Liu (Hangzhou Dianzi University, China), Dinghan Hu (Hangzhou Dianzi University, China), Huanqiang Zeng (Huaqiao University, China), Jiuwen Cao (Hangzhou Dianzi University, China)

ID2295: An Optimization-Based Approach to One-Bit Quantization

Florian Mayer (FH JOANNEUM Gesellschaft mbH, University of Applied Sciences, Austria), Christian Vogel (FH JOANNEUM Gesellschaft mbH, University of Applied Sciences, Austria)

ID1890: Deep Learning Method for Doppler Disambiguation
Marco Braun (University of Wuppertal, Germany), Adrian Becker (Aptiv PLC, Germany), Mirko Meuter (Aptiv PLC, Germany), Simon Roesler (Aptiv PLC, Germany), Kevin Kollek (University of Wuppertal, Germany), Anton Kummert (University of Wuppertal, Germany)

ID1410: Noise Decomposition Based on VGG and LSTM Networks
Yanze Zheng (University of Electronic Science and Technology of China, China), Yi Zhang (University of Electronic Science and Technology of China, China), Naixin Zhou (University of Electronic Science and Technology of China, China), Shibo Chen (University of Electronic Science and Technology of China, China), Yijiu Zhao (University of Electronic Science and Technology of China, China)

4:00 pm – 5:30 pm
B3L-01 High Frequency PLLs & Oscillators
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Aquarius 1
ORAL
Session Chair(s): Jose de la Rosa (Institute of Microelectronics of Seville), Xi Zhu (University of Technology Sydney)

4:00 pm
ID1051: A 28 nm 8.2-11.1 GHz Class-C Digitally Controlled Oscillator with 40 kHz Tuning Resolution
Lantao Wang (RWTH Aachen University, Germany), Johannes Bastl (RWTH Aachen University, Germany), Tim Lauber (RWTH Aachen University, Germany), Kenny Vohl (RWTH Aachen University, Germany), Jonas Meier (NXP Semiconductors, Germany), Andreas Köllmann (NXP Semiconductors, Germany), Ulrich Möhlmann (NXP Semiconductors, Germany), Michael Hanhart (RWTH Aachen University, Germany), Ralf Wunderlich (RWTH Aachen University, Germany), Stefan Heinen (RWTH Aachen University, Germany)

4:18 pm
ID1437: Back-Gate Coupling Technique for Phase Error Correction in PLL-Based Quadrature VCOs
Bahram Jafari (University of British Columbia, Canada), Shahriar Mirabbasi (University of British Columbia, Canada)

4:36 pm
ID1950: A 30.5-to-31 GHz Sampling PLL with Double-Edge Sampling PD and Implict Common-Mode VCO Scoring 39.69-fs RMS Jitter and -253.6-dB FoM in a 0.047mm² Area
Zhicheng Dong (Xidian University, China), Xiaoteng Zhao (Xidian University, China), Weitan Huang (Xidian University, China), Yuan Gao (Xidian University, China), Depeng Sun (Xidian University, China), Shubin Liu (Xidian University, China), Lihong Yang (Xidian University, China), Zhangming Zhu (Xidian University, China)

4:54 pm
ID2260: 28 GHz VCO Using Magnetically Tuning Trifilar Transformer in Cryogenic CMOS Application
Tai Jung Hsu (National Cheng Kung University, Taiwan), Jhih Hao Hong (National Cheng Kung University, Taiwan), Kuang Wei Cheng (National Cheng Kung University, Taiwan)

5:12 pm
ID2159: **A 24.6-29.6GHz Hybrid Sub-Sampling PLL with Tri-State Integral Path Achieving 44fs Jitter and -254.8dB FOM in 28nm CMOS**
Zhongkai Wang (University of California, Berkeley, United States), Minsoo Choi (Samsung Semiconductor, Inc, United States), Paul Kwon (University of California, Berkeley, United States), Zhaokai Liu (University of California, Berkeley, United States), Bozhi Yin (University of California, Berkeley, United States), Kyoungtae Lee (University of California, San Francisco, United States), Kwanseo Park (University of California, Berkeley, United States), Ayan Biswas (University of California, Berkeley, United States), Jaeduk Han (Hanyang University, Korea), Sijun Du (Delft University of Technology, Netherlands), Elad Alon (University of California, Berkeley, United States)

4:00 pm – 5:30 pm
B3L-02 ADC Circuit Techniques
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Aquarius 2
ORAL
Session Chair(s): Jorge Fernandes (INESC-ID / Instituto Superior Técnico), Ankesh Jain (IIT Delhi)

4:00 pm
ID2411: **A Dithered-Digital-Mixing Background Timing-Skew Calibration Method for Time-Interleaved ADCs**
Yunsong Tao (Tsinghua University, China), Yi Zhong (Tsinghua University, China), Jin Shao (Beijing Smart-Chip Microelectronics Technology Co. Ltd., China), Changyou Men (Hangzhou Vango Technologies, Inc., China), Lu Jie (Tsinghua University, China), Nan Sun (Tsinghua University, China)

4:18 pm
ID1649: **A High Dynamic Range Feedback Compensation Front-End for Unlimited Sampling ASDM ADC**
Binqiang Dan (Fuzhou University, China), Hui Qian (Fuzhou University, China), Zhongfeng Wang (Sun Yat-sen University, China)

4:36 pm
ID1851: **A 12.7 Bit Accurate and 5.3 nJ·μV2·ns Comparator with Dynamic-cum-Body Bias Technique in SOI**
Saurabh Dhiman (Indian Institute of Technology Mandi, India), Hitesh Shrimali (Indian Institute of Technology Mandi, India)

4:54 pm
ID1173: **An Improved Foreground Calibration Method for Capacitor Mismatch in NS-SAR ADC**
Jianzheng Li (Fudan University, China), Yuchen Zhao (Fudan University, China), Weimin Hu (Fudan University, China), Yufei Liu (Fudan University, China), Ziwei Liu (Fudan University, China), Yajie Qin (Fudan University, China)

5:12 pm
ID1566: **Analysis and Design of Constant-Slope Voltage-to-Time Converters**
Santeri Porrasmaa (Aalto University, Finland), Okko Järvinen (Aalto University, Finland), Ilia Kempi (Aalto University, Finland), Kari Stadius (Aalto University, Finland), Marko Kosunen (Aalto University, Finland), Jussi Ryynänen (Aalto University, Finland)

4:00 pm – 5:30 pm
B3L-03 Advanced Memory & Computing-in-Memory Circuits II

TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Aquarius 3
ORAL
Session Chair(s): Bo Wang (SUTD), Mircea Stan (University of Virginia)

4:00 pm
ID1977: Transposable Memory Based on the Ferroelectric Field-Effect Transistor
Jianze Wang (National University of Singapore, Singapore), Wei Zhang (National University of Singapore, Singapore), Zhen Wu (National University of Singapore, Singapore), Yimin Wang (National University of Singapore, Singapore), Leming Jiao (National University of Singapore, Singapore), Xiaolin Wang (National University of Singapore, Singapore), Xiao Gong (National University of Singapore, Singapore), Xuanyao Fong (National University of Singapore, Singapore)

4:18 pm
ID1383: An Efficient 6TP SRAM-Based CIM Macro with Column ADCs for Binarized Neural Networks (TCAS-II paper)
Ikramullah Shah (Hong Kong University of Science and Technology, Hong Kong), Khawar Sarfraz (Hong Kong University of Science and Technology, Hong Kong), Mansun Chan (Hong Kong University of Science and Technology; AI Chip Center for Emerging Smart System, Hong Kong

4:36 pm
ID1189: A 10T SRAM with Two Read and Write Modes Across Row and Column for CAM Operation and Computing In-Memory
Zhang Zhang (Hefei University of Technology, China), Zhihao Chen (Hefei University of Technology, China), Sikai Chen (Hefei University of Technology, China), Guangjun Xie (Hefei University of Technology, China), Jianmin Zeng (Shanghai Jiao Tong University, China), Gang Liu (Shanghai Jiao Tong University, China)

4:54 pm
ID1273: CIMR-V: An End-to-End SRAM-Based CIM Accelerator with RISC-V for AI Edge Device
Yan-Cheng Guo (National Yang Ming Chiao Tung University, Taiwan), Tian Sheuan Chang (National Yang Ming Chiao Tung University, Taiwan), Chih-Sheng Lin (Industrial Technology Research Institute, Taiwan), Bo-Cheng Chiou (Industrial Technology Research Institute, Taiwan), Chih-Ming Lai (Industrial Technology Research Institute, Taiwan), Shyh-Shyuan Sheu (Industrial Technology Research Institute, Taiwan), Wei-Chung Lo (Industrial Technology Research Institute, Taiwan), Shih-Chieh Chang (Industrial Technology Research Institute, Taiwan)

5:12 pm
ID1973: A 1Mb RRAM Macro with 9.8ns Read Access Time Utilizing Dynamic Reference Voltage for Reliable Sensing Operation (TCAS-II paper)
Junjie Mu (Nanyang Technological University, Singapore), Lu Lu (Nanyang Technological University, Singapore), Ju Eon Kim (Samsung Electronics Co., Ltd., Korea), Byungkwon An (Nanyang Technological University, Singapore), Vishal Sharma (Intel Technology India Pvt. Ltd., India), Arya Jagath Lekshmi (Nanyang Technological University, Singapore), Putu Andhita Dananjaya (Nanyang Technological University, Singapore), Weng Hong Lai (Nanyang Technological University, Singapore), Wen Siang Lew (Nanyang Technological University, Singapore), Tony Tae-Hyoung Kim (Nanyang Technological University, Singapore)

4:00 pm – 5:30 pm
B3L-04 Digital Circuits, Systems & Architecture for Machine Learning IV
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Aquarius 4

ORAL
Session Chair(s): Boris Vaisband (McGill University), Anh Tuan Do (IME, A*STAR)

4:00 pm
ID1284: Low-Latency Buffering for Mixed-Precision Neural Network Accelerator with MulTAP and FQPipe
Yike Li (Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences, China), Zheng Wang (Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences, China), Wenhui Ou (Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences, China), Chen Liang (Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences, China), Weiyu Zhou (Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences, Xidian University, China), Yongkui Yang (Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences, China), Chao Chen (Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences, China)

4:18 pm
ID2363: Hybrid-Grained Pruning and Hardware Acceleration for Convolutional Neural Networks
Yu Li (Shanghai University, China), Shan Cao (Shanghai University, China), Beining Zhao (Shanghai University, China), Wei Zhang (Shanghai University, China), Zhiyuan Jiang (Shanghai University, China)

4:36 pm
ID2039: An FPGA-Based Reconfigurable Accelerator for Convolution-Transformer Hybrid EfficientViT
Haikuo Shao (Nanjing University, China), Huihong Shi (Nanjing University, China), Wendong Mao (Sun Yat-sen University, China), Zhongfeng Wang (Nanjing University, China)

4:54 pm
ID2386: A 28.6 mJ/iter Stable Diffusion Processor for Text-to-Image Generation with Patch Similarity-Based Sparsity Augmentation and Text-Based Mixed-Precision Jiwon Choi (Korea Advanced Institute of Science and Technology, Korea), Wooyoung Jo (Korea Advanced Institute of Science and Technology, Korea), Seongyon Hong (Korea Advanced Institute of Science and Technology, Korea), Beomseok Kwon (Korea Advanced Institute of Science and Technology, Korea), Wonhoon Park (Korea Advanced Institute of Science and Technology, Korea), Hoi-Jun Yoo (Korea Advanced Institute of Science and Technology, Korea)

5:12 pm
ID2240: A Flexible and High-Precision Activation Function Unit Based on Equi-Error Partitioning Algorithm
Zelong Yuan (Shanghai Jiao Tong University, China), Siwei Yuan (Shanghai Jiao Tong University, China), Pengyu Liu (Shanghai Jiao Tong University, China), Chen Yin (Shanghai Jiao Tong University, China), Lei Xu (Shanghai Jiao Tong University, China), Weiguang Sheng (Shanghai Jiao Tong University, China), Naifeng Jing (Shanghai Jiao Tong University, China)

4:00 pm – 5:30 pm
B3L-05 6G, IoT Systems & Sensor Networks I
TRACK 3: COMMUNICATIONS CIRCUITS AND SYSTEMS

Venue: Gemini 1
ORAL
Session Chair(s): Susanto Rahardja (Northwestern Polytechnical University), Shan Cao (Shanghai Unviersity)

4:00 pm
ID1328: **A K-Band Eight-Element Dual-Beam Receiver with Current-Sharing-Based Low-Power Technique for LEO SATCOM in 65-nm CMOS**
Botao Yang (Zhejiang University, China), Nayu Li (Donghai Laboratory, Zhejang University, China), Yiwei Liu (Zhejiang University, China), Hang Lu (Zhejiang University, China), Ying Zhan (Zhejiang University, China), Chunyi Song (Donghai Laboratory, Zhejang University, China), Zhiwei Xu (Zhejiang University, China)

4:18 pm
ID1782: **Low Complexity Deep Learning Aided Channel Estimation Architecture for Vehicular Networks**
Asrar Ul Haq Syed (Indraprastha Institute of Information Technology, Delhi, India), Sumit Darak (Indraprastha Institute of Information Technology, Delhi, India), Abdul Karim Gizzini (Center for Digital Systems, IMT Nord Europe, Institut Mines-Télécom, University of Lille, France)

4:36 pm
ID2334: **A Low-Latency and High-Performance SCL Decoder with Frame-Interleaving**
Leyu Zhang (University of Science and Technology of China, China), Yuqing Ren (École Polytechnique Fédérale de Lausanne, Switzerland), Yifei Shen (École Polytechnique Fédérale de Lausanne, Switzerland), Wuyang Zhou (University of Science and Technology of China, China), Alexios Balatsoukas-Stimming (Eindhoven University of Technology, Netherlands), Chuan Zhang (Southeast University, China), Andreas Burg (École Polytechnique Fédérale de Lausanne, Switzerland)

4:54 pm
ID1054: **Machine Learning with Real-Time and Small Footprint Anomaly Detection System for In-Vehicle Gateway**
Yi Wang (Continental Automotive Singapore Pte. Ltd, Singapore), Yuanjin Zheng (Nanyang Technological University, Singapore), Yajun Ha (ShanghaiTech University, China)

5:12 pm
ID1229: **A Fully Integrated NB-IoT Wake-Up Receiver Utilizing an Optimized OFDM 12-Point FFT Wake-Up Engine**
Trevor Odelberg (University of Michigan, United States), Jaeho Im (University of Michigan, United States), Milad Moosavifar (University of Michigan, United States), David Wentzloff (University of Michigan, United States)

4:00 pm – 5:30 pm
B3L-06 High-Efficiency Power Converters & Drive Circuits
TRACK 4: POWER AND ENERGY CIRCUITS AND SYSTEMS

Venue: Gemini 2
ORAL
Session Chair(s): Dimitri Galayko (Sorbonne University), Yang Jiang (University of Macau)

4:00 pm
ID1239: **Design of Wireless In-Wheel Motor Drive with S/CP Compensation**
Xin Felix Chen (City University of Hong Kong, Hong Kong), Chi Kong Tse (City University of Hong Kong, Hong Kong), Qianhong Chen (Nanjing University of Aeronautics and Astronautics, China)

4:18 pm
ID1758: **A 24/48V to 0.8V-1.2V All-Digital Synchronous Buck Converter with Package-Integrated GaN Power FETs and 180nm Silicon Controller IC**

Kaushik Bhattacharyya (C. V. Raman Global University, India), Minxiang Gong (Intel Corporation, United States), Muya Chang (Nvidia Corporation, United States), Xin Zhang (IBM, United States), Arijit Raychowdhury (Georgia Institute of Technology, United States)

4:36 pm
ID1763: Miniaturized Solid-State Battery-Based DC-DC Switched Converter
Emeric Perez (Université Grenoble Alpes, CEA-Leti, France), Carlos Augusto-Berlitz (Université Grenoble Alpes, CEA-Leti, France), Yasser Moursy (Université Grenoble Alpes, CEA-Leti, France), Sami Oukassi (Université Grenoble Alpes, CEA-Leti, France), Bruno Allard (Laboratoire Ampère, INSA Lyon, France), Gaël Pillonnet (Université Grenoble Alpes, CEA-Leti, France)

4:54 pm
ID2011: A 12V-to-1V Outphase-Interleaved SC Hybrid Converter with Enhanced Inductor De-Energizing Slew Rate and Adaptive Deadtime Control (TCAS-II paper)
Xiongjie Zhang (University of Macau, Macau), Xinman Li (University of Macau, Macau), Anyang Zhao (University of Macau, Macau), Yang Jiang (University of Macau, Macau), Weihang Zhang (Xidian University, China), Jincheng Zhang (Xidian University, China), Rui Paulo Da Silva Martins (University of Macau, Macau), Pui-In Mak (University of Macau, Macau)

5:12 pm
ID2588: A Single-Inductor 5:1 Resonant Switched-Capacitor Ladder Converter with Continuous Voltage Conversion Capability
Sandeep Reddy Kukunuru (University of California, Santa Barbara, United States), Farzan Rezaei (University of California, Santa Barbara, United States), Loai G. Salem (University of California, Santa Barbara, United States)

4:00 pm – 5:30 pm
B3L-07 Deep Learning in Multimedia Applications
TRACK 12: MULTIMEDIA SYSTEMS AND APPLICATIONS

Venue: Pisces 1
ORAL
Session Chair(s): Ngai-Man Cheung (Singapore University of Technology and Design), Yiling Xu (Shanghai Jiao Tong University)

4:00 pm
ID1280: ASAUN-CS: Adaptive Stage Activated Unfolding Network for Compressive Sensing
Jian Yang (Hosei University, Japan), Kun Xiang (Hosei University, Japan), Haixin Wang (Hosei University, Japan), Yibo Fan (Fudan University, China), Jinjia Zhou (Hosei University, Japan)

4:18 pm
ID1449: Visual Question Answering Based Evaluation Metrics for Text-to-Image Generation
Mizuki Miyamoto (Hosei University, Japan), Ryugo Morita (Hosei University, Japan), Jinjia Zhou (Hosei University, Japan)

4:36 pm
ID1488: Generalized Few-Shot 3D Point Cloud Segmentation
Shuqian Yang (Nanyang Technological University, Singapore), Henghui Ding (Nanyang Technological University, Singapore), Xudong Jiang (Nanyang Technological University, Singapore)

4:54 pm
ID1783: ARC: Adaptive Rounding and Clipping Considering Gradient Distribution for Deep Convolutional Neural Network Training

Dahun Choi (Seoul National University of Science and Technology, Korea), Hyun Kim (Seoul National University of Science and Technology, Korea)

5:12 pm
ID2252: **Density Estimation-Based Effective Sampling Strategy for Neural Rendering**
Yunxiang He (ShanghaiTech University, China), Xin Lou (ShanghaiTech University, China)

4:00 pm – 5:30 pm
B3L-08 Neuromorphic Spiking Learning Systems & Applications II
TRACK 8: NEURAL NETWORKS AND NEUROMORPHIC ENGINEERING

Venue: Pisces 2
ORAL
Session Chair(s): Hailong Jiao (Peking University), Zhongrui Wang (Hongkong University)

4:00 pm
ID2560: **TSCM: A TCAM-Based Sparse Connection Memory Architecture in Neuromorphic Computing System for Cortical Simulation**
Fanxi Yang (Fudan University, China), Yuhan He (Fudan University, China), Ning Ma (Guangdong Institute of Intelligence Science and Technology, China), Lirong Zheng (Fudan University, China), Zhuo Zou (Fudan University, China)

4:18 pm
ID1525: **SPAT: FPGA-Based Sparsity-Optimized Spiking Neural Network Training Accelerator with Temporal Parallel Dataflow**
Yuanyuan Jiang (Peking University, China), Li Lun (Peking University, China), Jiawei Wang (Peking University, China), Mingqi Yin (Peking University, China), Hanqing Liu (Peking University, China), Zhenhui Dai (Peking University, China), Xiaole Cui (Peking University, China), Xiaoxin Cui (Peking University, China)

4:36 pm
ID1657: **Spiking Auto-Encoder Using Error Modulated Spike Timing Dependant Plasticity**
Ben Walters (James Cook University, Australia), Zhengyu Cai (University of Toronto, Canada), Hamid Rahimian Kalatehbali (York University, Canada), Amirali Amirsoleimani (York University, Canada), Roman Genov (University of Toronto, Canada), Jason Eshraghian (University of California, Santa Cruz, United States), Mostafa Rahimi Azghadi (James Cook University, Australia)

4:54 pm
ID2423: **Two-Step Spike Encoding Scheme and Architecture for Highly Sparse Spiking-Neural-Network**
Sangyeob Kim (Korea Advanced Institute of Science and Technology, Korea), Sangjin Kim (Korea Advanced Institute of Science and Technology, Korea), Soyeon Um (Korea Advanced Institute of Science and Technology, Korea), Soyeon Kim (Korea Advanced Institute of Science and Technology, Korea), Hoi-Jun Yoo (Korea Advanced Institute of Science and Technology, Korea)

5:12 pm
ID1401: **Accelerating BPTT-Based SNN Training with Sparsity-Aware and Pipelined Architecture**
Chaoming Fang (Westlake University, China), Fengshi Tian (Hong Kong University of Science and Technology, Hong Kong), Jie Yang (Westlake University, China), Mohamad Sawan (Westlake University, China)

4:00 pm – 5:30 pm
B3L-09 Signal Processing for Sensor Arrays & Networks
TRACK 10: DIGITAL SIGNAL PROCESSING

Venue: Pisces 3
ORAL
Session Chair(s): Qing Shen (Beijing Institute of Technology), Yun Chen (Fudan University)

4:00 pm
ID1147: A New Method for Source Number Estimation in the Presence of Unknown Nonuniform Noise
Mengxia He (University of Hong Kong, Hong Kong), Shing-Chow Chan (University of Hong Kong, Hong Kong)

4:18 pm
ID1865: 2-D Wideband DOA Estimation with Circular Arrays Based on the Difference Co-Array Concept
Hantian Wu (Beijing Institute of Technology, China), Qing Shen (Beijing Institute of Technology, China), Wei Liu (Queen Mary University of London, United Kingdom), Zheng Fu (Beijing Institute of Technology, China), Chenxi Liao (Beijing Institute of Technology, China)

4:36 pm
ID1999: A Low-Footprint FFT Accelerator for a RISC-V-Based Multi-Core DSP in FMCW Radars
Hector Andres Gonzalez Diaz (Technische Universität Dresden, Germany), Marco Stolba (Technische Universität Dresden, Germany), Bernhard Vogginger (Technische Universität Dresden, Germany), Tim Rosmeisl (Technische Universität Dresden, Germany), Chen Liu (Technische Universität Dresden, Germany), Christian Mayr (Technische Universität Dresden, Germany)

4:54 pm
ID2303: A Simulated Annealing Based Approach for Near-Optimal Sensor Selection in TDOA Localization System
Buyuan Zhu (Nanyang Technological University, Singapore), Qinglai Liu (Nanyang Technological University, Singapore), Saihua Xu (Nanyang Technological University, Singapore), Zhiping Lin (Nanyang Technological University, Singapore)

5:12 pm
ID1021: A Generalized Heat Kernel Smoothing Filter for Signal Denoising Over Graph
Chien-Cheng Tseng (National Kaohsiung University of Science and Technology, Taiwan), Su-Ling Lee (Chang-Jung Christian University, Taiwan)

4:00 pm – 5:30 pm
B3L-10 Emerging Technologies in Neural Prosthetic & Bio-inspired Devices
TRACK 14: SPECIAL SESSION

Venue: Pisces 4
ORAL
Session Chair(s): Hiroyuki Torikai (Hosei University, Japan), Hirro Sekiya (Chiba University)

4:00 pm
ID2199: A New Motor-Neuron Circuit Implementation
Paolo Arena (Università degli studi di Catania, Italy), Carlo Famoso (Università degli studi di Catania, Italy), Alessia Li Noce (Università degli studi di Catania, Italy), Alberto Motta (Università degli studi di Catania, Italy), Igor Galati (STMicroelectronics, Italy), Luca Patanè (Università degli studi di Messina, Italy)

4:18 pm
ID2268: **A Novel Hardware-Efficient Wireless Functional Electrical Stimulation Device Based on Nonlinear Dynamics of Ergodic Cellular Automaton**
Yunosuke Takemae (Hosei University, Japan), Hiroyuki Torikai (Hosei University, Japan), Masaya Kudo (Hosei University, Japan), Koki Sone (Hosei University, Japan)

4:36 pm
ID2269: **A Novel Ergodic Cellular Automaton Asthma Model: Reproductions of Nonlinear Dynamics of Asthma and Efficient FPGA Implementation**
Isaki Yamamoto (Hosei University, Japan), Hiroyuki Torikai (Hosei University, Japan)

4:54 pm
ID2167: **Investigation of Influence of APCMA-Based Wireless Communication on Neural Computation in Wireless Spiking Neural Networks**
Naoki Wakamiya (Osaka University, Japan)

5:12 pm
ID2350: **SNN Modeling of Cricket Auditory Network with Izhikevich Model Optimized by PSO**
Jiaying Lin (Chiba University, Japan), Ryuji Nagazawa (Chiba University, Japan), Koichi Tokunaga (Chiba University, Japan), Kien Nguyen (Chiba University, Japan), Hiroyuki Torikai (Hosei University, Japan), Won-Joo Hwang (Pusan National University, Korea), Hiroo Sekiya (Chiba University, Japan)

4:00 pm – 5:30 pm
B3L-11 Emerging Non-Volatile Devices for Computing
TRACK 14: SPECIAL SESSION

Venue: Virgo 1
ORAL
Session Chair(s): Sahil Shah (University of Maryland, College Park), Aishwarya Natarajan (Hewlett Packard Labs)

4:00 pm
ID1623: **An In-Memory Power Efficient Computing Architecture with Emerging VGSOT MRAM Device**
Md Rubel Sarkar (Virginia Polytechnic Institute and State University, United States), Shirazush Salekin Chowdhury (Virginia Polytechnic Institute and State University, United States), Jeffrey Sean Walling (Virginia Polytechnic Institute and State University, United States), Cindy Yang Yi (Virginia Polytechnic Institute and State University, United States)

4:18 pm
ID1634: **HfO2-Based Synaptic Spiking Neural Network Evaluation to Optimize Design and Testing Cost**
Snb Tushar (University of Tennessee, United States), Hritom Das (University of Tennessee, United States), Garrett S. Rose (University of Tennessee, United States)

4:36 pm
ID1667: **On-Chip Adaptation for Reducing Mismatch in Analog Non-Volatile Device Based Neural Networks**
Charana Sonnadara (University of Maryland, United States), Sahil Shah (University of Maryland, United States)

4:54 pm
ID2331: Design of High-Performance and Compact CAM for Supporting Data-Intensive Applications
Liu Liu (University of Notre Dame, United States), Ann Franchesca Laguna (De La Salle University, Philippines), Michael Niemier (University of Notre Dame, United States), Xiaobo Sharon Hu (University of Notre Dame, United States)

5:12 pm
ID2575: Memristive Quaternary Content-Addressable Memories for Implementing Boolean Functions
Luca Buonanno (Hewlett Packard Enterprise, United States), Giacomo Pedretti (Hewlett Packard Enterprise, United States), Lei Zhao (Hewlett Packard Enterprise, United States), Aishwarya Natarajan (Hewlett Packard Enterprise, United States), Todd Richmond (Hewlett Packard Enterprise, United States), John Moon (Hewlett Packard Enterprise, United States), Rand Jean (Hewlett Packard Enterprise, United States), Xia Sheng (Hewlett Packard Enterprise, United States), Ron Roth (Hewlett Packard Enterprise, United States), Jim Ignowski (Hewlett Packard Enterprise, United States)

4:00 pm – 5:30 pm
B3L-12 Technology & Agribusiness
TRACK 14: SPECIAL SESSION

Venue: Virgo 2
ORAL
Session Chair(s): Victor Grimblatt (Synopsys), Danilo Demarchi (Politecnico di Torino)

4:00 pm
ID2162: Agriculture Impact on Climate Change and Climate Change Impact on Agriculture - Low Power Design
Victor Grimblatt (Synopsys, Inc., Chile)

4:18 pm
ID1954: High-Throughput Starch Content Estimation Using RF Return Loss: Theory, Analysis and Test Instrument Design
Temitope Odedeyi (University College London, United Kingdom), Ali Issa (University College London, United Kingdom), Clive Poole (University College London, United Kingdom), Izzat Darwazeh (University College London, United Kingdom)

4:36 pm
ID2103: An Energy Autonomous and Battery-Free Plant's Electrical Impedance Measurement System
Stefano Calvo (Politecnico di Torino, Italy), Mattia Barezzi (Politecnico di Milano, Italy), Umberto Garlando (Politecnico di Torino, Italy), Roberto La Rosa (STMicroelectronics, Italy), Danilo Demarchi (Politecnico di Torino, Italy)

4:54 pm
ID2201: A Wireless Biosensor Node for Real-Time Crop Monitoring in Precision Agriculture
Andrea Boni (University of Parma, Italy), Edoardo Graiani (University of Parma, Italy), Valentina Bianchi (University of Parma, Italy), Ilaria De Munari (University of Parma, Italy), Michele Caselli (University of Parma, Italy)

5:12 pm
ID2440: Net Fishing Localization: Performance of TDOA-Based Positioning Technique in Underwater Acoustic Channels Using Chirp Signals

Marwane Rezzouki (ESTIA Institute of Technology, France), Guillaume Ferré (Université de Bordeaux, IMS Laboratory & Bordeaux INP, France), Guillaume Terrasson (ESTIA Institute of Technology, France), Alvaro Llaria (ESTIA Institute of Technology, France)

4:00 pm – 5:30 pm
B3L-13 Physical Hardware Evaluation from Design Trust to System Reliability
TRACK 14: SPECIAL SESSION

Venue: Virgo 3
ORAL
Session Chair(s): Deruo Cheng (Nanyang Technological University), Gwee Bah Hwee (Nanyang Technological University)

4:00 pm
ID2099: MLConnect: A Machine Learning Based Connection Prediction Framework for Error Correction in Recovered Circuit
Xuenong Hong (Nanyang Technological University, Singapore), Zilong Hu (Nanyang Technological University, Singapore), Han Zhang (Nanyang Technological University, Singapore), Yee-Yang Tee (Nanyang Technological University, Singapore), Tong Lin (Nanyang Technological University, Singapore), Yiqiong Shi (Nanyang Technological University, Singapore), Deruo Cheng (Nanyang Technological University, Singapore), Bah-Hwee Gwee (Nanyang Technological University, Singapore)

4:18 pm
ID2111: A Strong 4×4 S-Box Using an Enhanced Tent Map
Phuc-Phan Duong (University of Electro-Communications, Japan), Trong-Thuc Hoang (University of Electro-Communications, Japan), Cong-Kha Pham (University of Electro-Communications, Japan)

4:36 pm
ID2358: A Novel Non-Profiling Side-Channel Attack on Masked Devices with Connectivity Matrix
Juncheng Chen (Nanyang Technological University, Singapore), Han Zhang (Nanyang Technological University, Singapore), Zishuo Yang (Nanyang Technological University, Singapore), Yicheng Xu (Nanyang Technological University, Singapore), Aung Kyaw Nay (Nanyang Technological University, Singapore), Kwen-Siong Chong (Zero-Error Systems Pte Ltd, Singapore), Zhiping Lin (Nanyang Technological University, Singapore), Bah-Hwee Gwee (Nanyang Technological University, Singapore)

4:54 pm
ID2116: An Efficient Hiding Countermeasure with Xilinx MMCM Primitive in Spread Mode
Thai-Ha Tran (University of Electro-Communications, Japan), Van-Phuc Hoang (Le Quy Don Technical University, Vietnam), Duc-Hung Le (Ho Chi Minh City University of Science, Vietnam), Trong-Thuc Hoang (University of Electro-Communications, Japan), Cong-Kha Pham (University of Electro-Communications, Japan)

5:12 pm
ID2547: Explainable Automated Data Estimation in Logic State Imaging of Embedded SRAM
Samuel Chef (Nanyang Technological University, Singapore), Chung Tah Chua (Nanyang Technological University, Singapore), Jing Yun Tay (Nanyang Technological University, Singapore), Chee Lip Gan (Nanyang Technological University, Singapore)

4:00 pm – 5:30 pm
Info Security Part 2

EMBEDDED WORKSHOP

Venue: Leo 1
Session Chair(s): Dr. Shivam Bhasin（NTU, Singapore)

4:00 pm – 5:30 pm
SW: CAS Standard Workshop on Digital Healthcare II
SPECIAL WORKSHOP

Venue: Virgo 4
Session Chair(s): Yongfu Li (Shanghai Jiao Tong University, China), Boon Chong Ang (Intel), Yang Zhao (Shanghai Jiao Tong University, China), Wei Mao (Xidian University, China), and Lian Yong (York University)

7:00 pm – 9:00 pm
Gala Dinner
SOCIAL EVENT

Venue: B2 Ballroom

Technical Program: Wednesday 22 May 2024

7:45 am – 9:00 am
Registration
Venue: Foyer of Taurus Room (Secretariat Room)

9:00 am – 12:30 pm
Autonomous Mobility CAS (AutoCAS)
EMBEDDED WORKSHOP

Venue: Leo 1
Session Chair(s): Kyung Ki Kim (Daegu University, Korea), Preet Yadav (NXP Semiconductors, India)

9:00 am – 12:30 pm
SW: 3D Integration & Advanced Packaging
SPECIAL WORKSHOP

Venue: Virgo 4
Session Chair(s): Do Anh Tuan (IME, A*STAR), Fong (Kelvin) Xuanyao (National University of Singapore)

9:00 am – 10:30 am
C1L-01 Voltage Regulators & Current Reference
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Aquarius 1
ORAL
Session Chair(s): Liheng Lou (University of Science and Technology of China), Xi Zhu (University of Technology Sydney)

09:00 am
ID1425: A Single-Point, Auto-Calibration Technique for PTAT/CTAT Resistance Based Current References
Arpan Jain (International Institute of Information Technology Hyderabad, India), Ashfakh Ali (International Institute of Information Technology Hyderabad, India), Dheekshith Akula (International Institute of Information Technology Hyderabad, India), Abhishek Pullela (International Institute of Information Technology Hyderabad, India), Zia Abbas (International Institute of Information Technology Hyderabad, India)

09:18 am
ID2498: A Fully Synthesizable Capacitorless Digital LDO for Distributed Power Delivery Network
Chengwei Cao (Fudan University, China), Yiwen Tang (Fudan University, China), Xiongchuan Huang (Fudan University, China), Zhuo Zou (Fudan University, China), Lirong Zheng (Fudan University, China)

09:36 am
ID1815: A Tri-Loop Fast-Transient Digital LDO with Adaptive-Gain Control and Fine-Loop Freezer

Muhammad Haris Farooq (National University of Sciences & Technology, Pakistan), Muhammad Abrar Akram (New York University Abu Dhabi, U.A.E.), Shirin Qaisar (National University of Sciences & Technology, Pakistan), Soon-Jae Kweon (Catholic University of Korea, Korea), Hammad M. Cheema (National University of Sciences & Technology, Pakistan), Sohmyung Ha (New York University Abu Dhabi, U.A.E.)

09:54 am
ID1818: An Analog-Assisted Fast-Transient Digital LDO with a Charge-Pump-Based Fine Loop Achieving 0.14-mV Output Voltage Ripples
Shirin Qaisar (National University of Sciences & Technology, Pakistan), Muhammad Abrar Akram (New York University Abu Dhabi, U.A.E.), Muhammad Haris Farooq (National University of Sciences & Technology, Pakistan), Soon-Jae Kweon (Catholic University of Korea, Korea), Hammad M. Cheema (National University of Sciences & Technology, Pakistan), Sohmyung Ha (New York University Abu Dhabi, U.A.E.)

10:12 am
ID2372: A High-Switching-Frequency Multi-Mode Four-Switch Buck-Boost Converter Empowered by a 400-MHz Bandwidth Two-Stage Operational Amplifier
Wangchen Fan (Southeast University, China), Qinsong Qian (Southeast University, China), Weifeng Sun (Southeast University, China), Zhongyuan Fang (Southeast University, China)

9:00 am – 10:30 am
C1L-02 Memory Circuits & Interconnects
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Aquarius 2
ORAL
Session Chair(s): Zunsong Yang (Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China.), Hui Wang (Shanghai Jiao Tong University)

09:00 am
ID2512: A Compact and Low-Power Column Readout Circuit Based on Digital Delay Chain
Minkyu Yang (Korea Advanced Institute of Science and Technology, Korea), Changjoo Park (Korea Advanced Institute of Science and Technology, Korea), Wanyeong Jung (Korea Advanced Institute of Science and Technology, Korea)

09:18 am
ID1688: A 0.2 pJ/Bit, Energy-Efficient, Half-Rate Hybrid Circuit Topology at 6-Gb/s in 1.2V, 65 nm CMOS
Prema Kumar Govindaswamy (Indian Institute of Technology Bhubaneswar, India), Mursina Khatun (Indian Institute of Technology Bhubaneswar, India), Vijay Shankar Pasupureddi (Indian Institute of Technology Bhubaneswar, India)

09:36 am
ID1723: A 0.77-pJ/Bit 40-Gb/s/pin Single-Ended Hybrid DAC-Based Transmitter for Memory Interfaces
Sanghyuk Seo (Seoul National University, Korea), Yong-Un Jeong (Sejong University, Korea), Jaekwang Yun (Seoul National University, Korea), Jaewook Kim (SK hynix Inc., Korea), Suhwan Kim (Seoul National University, Korea)

09:54 am
ID1836: A Wide-Range Reference-Less Digital Clock and Data Recovery for Harmonic-Lock-Free Frequency Acquisition

Hyun-Bin Lee (Seoul National University of Science and Technology, Korea), Yoon Heo (Seoul National University of Science and Technology, Korea), Won-Young Lee (Seoul National University of Science and Technology, Korea)

10:12 am
ID1022: Quantization-Robust On-Chip Jitter Measurement Technique for Multiple Local Oscillator Systems
Lukas Schramm (Intel Corporation, Germany), Peter Baumgartner (Intel Germany, Germany), Jasmin Aghassi-Hagmann (Karlsruhe Institute of Technology, Germany)

9:00 am – 10:30 am
C1L-03 SOC, NOC, Multi-Core, & 3D/2.5D Systems
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Aquarius 3
ORAL
Session Chair(s): Kun-Chih - Jimmy Chen (National Yang Ming Chiao Tung University), Fakhrul Zaman Rokhani (University Putra Malaysia)

09:00 am
ID1681: Exploring Error Correction Circuits on RISC-V Based Systems for Space Applications
Nazim Altar Koca (Nanyang Technological University, Singapore), Chip Hong Chang (Nanyang Technological University, Singapore), Anh Tuan Do (Institute of Microelectronics, Agency for Science, Technology and Research, Singapore), Vishnu Paramasivam Nambiar (Institute of Microelectronics, Agency for Science, Technology and Research, Singapore)

09:18 am
ID2306: Crosstalk and Power Analysis in Tapered Based Composite Cu-CNT TSV in 3D IC
Shivangi Chandrakar (International Institute of Information Technology Naya Raipur, India), Deepika Gupta (International Institute of Information Technology, Naya Raipur, India), Manoj Kumar Majumder (International Institute of Information Technology, Naya Raipur, India)

09:36 am
ID2194: An 2.31uJ/Inference Ultra-Low Power Always-on Event-Driven AI-IoT SoC with Switchable nvSRAM Compute-in-Memory Macro (TCAS-II paper)
Haoyang Sang (Korea Advanced Institute of Science and Technology, Korea), Wenao Xie (Korea Advanced Institute of Science and Technology, Korea), Gwangtae Park (Korea Advanced Institute of Science and Technology, Korea), Hoi-Jun Yoo (Korea Advanced Institute of Science and Technology, Korea)

09:54 am
ID1550: A Scalable Multi-Chip YOLO Accelerator with a Lightweight Inter-Chip Adapter
Jicheon Kim (Seoul National University, Korea), Chunmyung Park (Seoul National University, Korea), Eunjae Hyun (Seoul National University, Korea), Xuan Truong Nguyen (Seoul National University, Korea), Hyuk-Jae Lee (Seoul National University, Korea)

10:12 am
ID2299: 3D Partitioning with Pipeline Optimization for Low-Latency Memory Access in Many-Core SoCs
Sudipta Das (IMEC & Vrije Universiteit Brussel, Belgium), Samuel Riedel (ETH Zürich, Switzerland), Marco Bertuletti (ETH Zürich, Switzerland), Luca Benini (Integrated Systems Laboratory, ETH Zürich, Switzerland), Moritz Brunion (IMEC, Belgium), Julien Ryckaert (IMEC, Belgium), James

Myers (IMEC, United Kingdom), Dwaipayan Biswas (IMEC, Belgium), Dragomir Milojevic (IMEC & Université Libre de Bruxelles, Belgium)

9:00 am – 10:30 am
C1L-04 Circuit Techniques for Computing-in-Memory & Machine Learning
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Aquarius 4
ORAL
Session Chair(s): Shuenn-Yuh Lee (National Cheng Kung University, Taiwan), Mladen Berekovic (Universität zu Lübeck)

09:00 am
ID1201: A 19.7 TFLOPS/W Multiply-Less Logarithmic Floating-Point CIM Architecture with Error-Reduced Compensated Approximate Adder
Mengjie Li (Fudan University, China), Hongyi Zhang (Fudan University, China), Siqi He (Fudan University, China), Haozhe Zhu (Fudan University, China), Hao Zhang (China Mobile Limited, China), Jinglei Liu (China Mobile Limited, China), Jiayuan Chen (China Mobile Limited, China), Zhenping Hu (China Mobile Limited, China), Xiaoyang Zeng (Fudan University, China), Chixiao Chen (Fudan University, China)

09:18 am
ID2207: Reconfigurable Precision SRAM-Based Analog In-Memory-Compute Macro Design
Jinane Bazzi (King Abdullah University of Science and Technology, Saudi Arabia), Rachid Jamil (American University of Beirut, Lebanon), Dana ElHajj (American University of Beirut, Lebanon), Rouwaida Kanj (American University of Beirut, Lebanon), Mohammed Fouda (Rain Neuromorphics Inc., United States), Ahmed Eltawil (King Abdullah University of Science and Technology, Saudi Arabia)

09:36 am
ID2347: PVT-Insensitive Time-Domain-Based In-Memory Computation with Improved Linearity for Binary Neural Networks
Amandeep Singh (Indian Institute of Technology Roorkee, India), Bishnu Prasad Das (Indian Institute of Technology Roorkee, India)

09:54 am
ID2455: ACNNE: An Adaptive Convolution Engine for CNNs Acceleration Exploiting Partial Reconfiguration on FPGAs
Chun-Hsian Huang (National Taitung University, Taiwan), Shao-Wei Tang (National Chung Cheng University, Taiwan), Pao-Ann Hsiung (National Chung Cheng University, Taiwan)

10:12 am
ID1655: An Efficient Sparse-Aware Summation Optimization Strategy for DNN Accelerator
Danqing Zhang (Xi'an Jiaotong University, China), Baoting Li (Xi'an Jiaotong University, China), Hang Wang (Xi'an Jiaotong University, China), Xuchong Zhang (Xi'an Jiaotong University, China), Hongbin Sun (Xi'an Jiaotong University, China)

9:00 am – 10:30 am
C1L-05 Quantum Computing Circuits & Systems I
TRACK 5: BEYOND CMOS: NANOELECTRONICS AND HYBRID SYSTEMS INTEGRATION

Venue: Gemini 1
ORAL

Session Chair(s): Georgios Sirakoulis (Democritus University of Thrace), Vasileios Ntinas (TU Dresden)

09:00 am
ID1296: Formal Verification for Cyclic Quantum Walk Circuits
Benedicto Campbell (North Dakota State University, United States), Sudarshan Srinivasan (North Dakota State University, United States)

09:18 am
ID2119: Quantum Readout Processing Accelerator with a CORDIC Core at Cryogenic Temperature
Yi Sheng Chong (Institute of Microelectronics, Agency for Science, Technology and Research, Singapore), Hongyu Cao (Nanyang Technological University, Singapore), Wang Ling Goh (Nanyang Technological University, Singapore), Patrick Bore (Centre for Quantum Technologies, National University of Singapore, Singapore), Yuanzheng Paul Tan (Nanyang Technological University, Singapore), Yung Szen Yap (CSNano, Universiti Teknologi Malaysia, Malaysia), Rainer Dumke (Nanyang Technological University, Singapore), Vishnu Paramasivam Nambiar (Institute of Microelectronics, Agency for Science, Technology and Research, Singapore), Anh Tuan Do (Institute of Microelectronics, Agency for Science, Technology and Research, Singapore)

09:36 am
ID2216: An S-Band SiGe BiCMOS Transmitter for an NV Center Based Quantum Magnetometer
Hadi Lotfi (University of Stuttgart, Germany), Michal Kern (University of Stuttgart, Germany), Thomas Unden (NVision Imaging Technologies GmbH, Germany), Jochen Scharpf (NVision Imaging Technologies GmbH, Germany), Ilai Schwartz (NVision Imaging Technologies GmbH, Germany), Philipp Neumann (NVision Imaging Technologies GmbH, Germany), Jens Anders (University of Stuttgart, Germany)

09:54 am
ID2510: Circuit Partitioning for Multi-Core Quantum Architectures with Deep Reinforcement Learning
Arnau Pastor (Universitat Politècnica de Catalunya, Spain), Pau Escofet (Universitat Politècnica de Catalunya, Spain), Sahar Ben Rached (Universitat Politècnica de Catalunya, Spain), Eduard Alarcón (Universitat Politècnica de Catalunya, Spain), Pere Barlet-Ros (Universitat Politècnica de Catalunya, Spain), Sergi Abadal (Universitat Politècnica de Catalunya, Spain)

10:12 am
ID2550: A Cryogenic Phase-Selection Superconducting Qubit Controller with Envelope-Tracking in 28nm Bulk CMOS
Yanshu Guo (Nanyang Technological University, Singapore), Wenqiang Huang (Tsinghua University, China), Yaoyu Li (Tsinghua University, China), Tian Tian (Tsinghua University, China), Yange Wang (Nanyang Technological University, Singapore), Shiquan Wang (Nanyang Technological University, Singapore), Zhihua Wang (Tsinghua University, China), Hanjun Jiang (Tsinghua University, China), Yuanjin Zheng (Nanyang Technological University, Singapore)

9:00 am – 10:30 am
C1L-06 Education in Circuits & Systems I
TRACK 13: EDUCATION IN CIRCUITS AND SYSTEMS

Venue: Gemini 2
ORAL
Session Chair(s): Carlos Silva Cárdena (Pontificia Universidad Catolica del Peru), Izzet Kale (University of Westminster, UK)

09:00 am
ID1163: Research Experiences for Teachers on Chip Design
John Hu (Oklahoma State University, United States), James Stine (Oklahoma State University, United States), Wooyeol Choi (Seoul National University, Korea), Erin Dyke (Oklahoma State University, United States)

09:18 am
ID2041: Toward Scalable Laboratories in Signals and Systems: Content, Deployment, and Grading
Yousef Helal (University of California, Berkeley, United States), Naomi Sagan (University of California, Berkeley, United States), Drake Lin (University of California, Berkeley, United States), Anmol Parande (University of California, Berkeley, United States), Dominic Carrano (University of California, Berkeley, United States), Babak Ayazifar (University of California, Berkeley, United States)

09:36 am
ID2209: Incorporating Design Skills in an Introductory Electric Circuits Laboratory
Kevin Wine (Rutgers University, United States), Demetrios Lambropoulos (Rutgers University, United States), Laleh Najafizadeh (Rutgers University, United States), Sasan Haghani (Rutgers University, United States)

09:54 am
ID2341: On Various Extensions of the Shannon-Hagelbarger Concavity Theorem
Ibrahim Elfadel (Khalifa University, U.A.E.)

10:12 am
ID2359: Case Study: Understanding Internet Anomalies
Hardeep Kaur Takhar (Simon Fraser University, Canada), Luiz Felipe Oliveira (Simon Fraser University, Canada), Ljiljana Trajkovic (Simon Fraser University, Canada)

9:00 am – 10:30 am
C1L-07 Biomedical Circuits & Systems I
TRACK 6: BIOMEDICAL CIRCUITS AND SYSTEMS

Venue: Pisces 1
ORAL
Session Chair(s): Yuanjin Zheng (Nanyang Technological University, Singapore), Mohamad Sawan (Westlake University)

09:00 am
ID2393: A CMOS-Integrated 23.88-ppm/° C, 6.825-µW Voltage Reference with Offset-Self-Cancellation for Portable Biomedical Equipment Applications
Haonan Fan (Southeast University, China), Zhongyuan Fang (Southeast University, China), Minggang Chen (Southeast University, China), Weifeng Sun (Southeast University, China)

09:18 am
ID2121: A 72-Channel Resistive-Sensor Interface IC with High Energy Efficiency and a Wide Input Range
Sunglim Han (Korea Advanced Institute of Science and Technology, Korea), Hoyong Seong (Korea Advanced Institute of Science and Technology, Korea), Sein Oh (Korea Advanced Institute of Science and Technology, Korea), Jimin Koo (Korea Advanced Institute of Science and Technology, Korea), Hanbit Jin (Electronics and Telecommunications Research Institute, Korea), Hye Jin Kim (Electronics and Telecommunications Research Institute, Korea), Sohmyung Ha (New York

University Abu Dhabi, U.A.E.), Minkyu Je (Korea Advanced Institute of Science and Technology, Korea)

09:36 am
ID1390: A Low-Power Δ-ΔΣ-Based Bio-Impedance Readout IC with Capacitive-Feedback Baseline Cancellation
Haidam Choi (Korea Advanced Institute of Science and Technology, Korea), Ji-Hoon Suh (Korea Advanced Institute of Science and Technology, Korea), Gichan Yun (Korea Advanced Institute of Science and Technology, Korea), Sein Oh (Korea Advanced Institute of Science and Technology, Korea), Song-I Cheon (Korea Advanced Institute of Science and Technology, Korea), Sohmyung Ha (New York University Abu Dhabi, U.A.E.), Minkyu Je (Korea Advanced Institute of Science and Technology, Korea)

09:54 am
ID1788: A Biopotential Recording IC with <10-ms-Settling Hybrid DC Servo Loop
Yegeun Kim (Korea Advanced Institute of Science and Technology, Korea), Changhun Seok (Korea Advanced Institute of Science and Technology, Korea), Yoontae Jung (Korea Advanced Institute of Science and Technology, Korea), Sohmyung Ha (New York University Abu Dhabi, U.A.E.), Minkyu Je (Korea Advanced Institute of Science and Technology, Korea)

10:12 am
ID1862: A High-Throughput Impedance Measurement IC Using Synchronous Cyclic Integration Technique
Karam Ellahi (National University of Sciences & Technology, Pakistan), Soon-Jae Kweon (Catholic University of Korea, Korea), Asra Malik (National University of Sciences & Technology, Pakistan), Muhammad Abrar Akram (New York University Abu Dhabi, U.A.E.), Song-I Cheon (Korea Advanced Institute of Science and Technology, Korea), Yoontae Jung (Korea Advanced Institute of Science and Technology, Korea), Minkyu Je (Korea Advanced Institute of Science and Technology, Korea), Hammad M. Cheema (National University of Sciences & Technology, Pakistan), Sohmyung Ha (New York University Abu Dhabi, U.A.E.)

9:00 am – 10:30 am
C1L-08 Neuromorphic Systems I
TRACK 8: NEURAL NETWORKS AND NEUROMORPHIC ENGINEERING

Venue: Pisces 2
ORAL
Session Chair(s): Fernando Perez Peña (Universidad de Cádiz), Juan Pedro Domínguez Morales (Universidad de Sevilla)

09:00 am
ID2577: ASIC Implementation of Efficient 512-Neuron 256K-Synapses Digital Neuromorphic Processor with On-Chip Encoding in 22nmFDX
Ahmed Ghonem (Ohio State University, United States), Eslam Tawfik (Ohio State University, United States)

09:18 am
ID2357: PULSE: Parametric Hardware Units for Low-Power Sparsity-Aware Convolution Engine
Ilkin Aliyev (University of Arizona, United States), Tosiron Adegbija (University of Arizona, United States)

09:36 am
ID2054: **Co-Optimized Training of Models with Synaptic Delays for Digital Neuromorphic Accelerators**
Alberto Patiño-Saucedo (IMSE-CNM, CSIC & Universidad de Sevilla, Spain), Roy Meijer (IMEC, Netherlands), Paul Detteter (IMEC, Netherlands), Amirreza Yousefzadeh (IMEC, Netherlands), Laura Garrido-Regife (IMSE-CNM, CSIC & Universidad de Sevilla, Netherlands), Bernabé Linares-Barranco (IMSE-CNM, CSIC & Universidad de Sevilla, Spain), Manolis Sifalakis (IMEC, Netherlands)

09:54 am
ID2003: **An End-to-End SoC for Brain-Inspired CNN-SNN Hybrid Applications**
Zhaotong Zhang (Peking University, China), Yi Zhong (Peking University, China), Yingying Cui (Peking University, China), Yawei Ding (Peking University, China), Yukun Xue (Peking University, China), Qibin Li (Peking University, China), Ruining Yang (Peking University, China), Jian Cao (Peking University, China), Yuan Wang (Peking University, China)

10:12 am
ID1315: **Odour Localization in Neuromorphic Systems**
Thorben Schoepe (Forschungszentrum Jülich GmbH, Germany), Damien Drix (University of Hertfordshire, United Kingdom), Franz Marcus Schüffny (Technische Universität Dresden, Germany), Rebecca Miko (University of Hertfordshire, United Kingdom), Samuel Sutton (University of Hertfordshire, United Kingdom), Elisabetta Chicca (University of Groningen, Netherlands), Michael Schmuker (University of Hertfordshire, United Kingdom)

9:00 am – 10:30 am
C1L-09 Image Processing
TRACK 10: DIGITAL SIGNAL PROCESSING

Venue: Pisces 3
ORAL
Session Chair(s): Fengwei An (Southern University of Science and Technology), Xin Lou (ShanghaiTech University)

09:00 am
ID1167: **Memory-Based Contrastive Learning with Optimized Sampling for Incremental Few-Shot Semantic Segmentation**
Yuxuan Zhang (Tongji University, China), Miaojing Shi (King's College London & Tongji University, China), Taiyi Su (Tongji University, China), Hanli Wang (Tongji University, China)

09:18 am
ID1197: **A High-Throughput Lossless Image Compression Engine Optimized for Compression Ratio**
Siqi Cai (Shanghai Jiao Tong University, China), Yuzhou Chen (Shanghai Jiao Tong University, China), Wenhui Zhang (Shanghai Jiao Tong University, China), Zeyuan Jin (Shanghai Jiao Tong University, China), Gang Wang (Shanghai Jiao Tong University, China), Hao Chen (Shanghai Jiao Tong University, China), Guanghui He (Shanghai Jiao Tong University, China)

09:36 am
ID1215: **FIRNet: Forward-Inverse Reinforcement Network for Image Restoration Through Scattering Media**
Pengfei Qi (Nanyang Technological University, Singapore), Yi Wang (Continental Automotive Singapore Pte. Ltd, Singapore), Xue Feng (Laboratory of Flexible Electronics Technology, Tsinghua University, China), Yuanjin Zheng (Nanyang Technological University, Singapore)

09:54 am
ID1468: Unsupervised Image Enhancement via Contrastive Learning
Di Li (Northwestern Polytechnical University, China), Susanto Rahardja (Northwestern Polytechnical University & Singapore Institute of Technology, China)

10:12 am
ID1679: Tri-Directional Decoder for Edge Discontinuity Classification
Jiayue Wang (Seoul National University, Korea), Hyuk-Jae Lee (Seoul National University, Korea), Hansang Cho (Samsung Electro-Mechanics Co., Ltd., Korea), Byungsoo Kang (Samsung Electro-Mechanics Co., Ltd., Korea), Hyunmin Jung (Seoul National University of Science and Technology, Korea)

9:00 am – 10:30 am
C1L-10 Brain Computer Interface: Algorithm & Signal Processing
TRACK 14: SPECIAL SESSION

Venue: Pisces 4
ORAL
Session Chair(s): Yasue Mitsukura (Keio University), Yoshifumi Nishio (Tokushima University, Japan)

09:00 am
ID1524: A Probability Method to Estimate the State of a Digital Resonate-and-Fire Neuron Without Running a Simulation
Trung-Khanh Le (Ho Chi Minh City University of Science, Vietnam), Trong-Tu Bui (Ho Chi Minh City University of Science, Vietnam), Duc-Hung Le (Ho Chi Minh City University of Science, Vietnam)

09:18 am
ID2375: Feature Extraction of Neuronal Activity by Attractor Reconstruction in Neural Networks with Delayed Couplings
Yoko Uwate (Tokushima University, Japan), Marie Obien (MaxWell Biosystems, Switzerland), Urs Frey (MaxWell Biosystems, Switzerland), Yoshifumi Nishio (Tokushima University, Japan)

09:36 am
ID2540: FewShotEEG Learning and Classification for Brain-Computer Interface
Subrato Bharati (Concordia University, Canada), M. Omair Ahmad (Concordia University, Canada), M.N.S. Swamy (Concordia University, Canada)

09:54 am
ID1868: EEG Emotion Recognition Based on Dynamic Graph Neural Networks
Yi Guo (Xi'an Jiaotong University, China), Chao Tang (Xi'an Jiaotong University, China), Hao Wu (Xi'an University of Technology, China), Badong Chen (Xi'an Jiaotong University, China)

10:12 am
ID2396: On Optimizing Deep Neural Networks Inference on CPUs for Brain-Computer Interfaces Using Inference Engines
Okba Bekhelifi (Intelligent Systems Research Laboratory LARESI, University of Sciences and Technology of Oran-Moha, Algeria), Nasr-Eddine Berrached (Intelligent Systems Research Laboratory LARESI, University of Sciences and Technology of Oran-Moha, Algeria)

9:00 am – 10:30 am
C1L-11 Improving the Accuracy & Reliability of Analog-Based In-Memory Computing Systems I

TRACK 14: SPECIAL SESSION

Venue: Virgo 1
ORAL
Session Chair(s): Corey Lammie (IBM Research - Zurich), Jason K. Eshraghian (University of California, Santa Cruz)

09:00 am
ID1283: Improving the Accuracy of Analog-Based In-Memory Computing Accelerators Post-Training
Corey Lammie (IBM Research - Zürich, Switzerland), Athanasios Vasilopoulos (IBM Research - Zürich, Switzerland), Julian Büchel (IBM Research - Zürich, Switzerland), Giacomo Camposampiero (IBM Research - Zürich, Switzerland), Manuel Le Gallo (IBM Research - Zürich, Switzerland), Malte Rasch (IBM T. J. Watson Research Center, United States), Abu Sebastian (IBM Research - Zürich, Switzerland)

09:18 am
ID1615: Coincidence Detection with an Analog Spiking Neuron Exploiting Ferroelectric Polarization
Paolo Gibertini (NaMLab gGmbH, Germany), Luca Fehlings (NaMLab gGmbH, Germany), Thomas Mikolajick (NaMLab gGmbH, Technical University of Dresden, Germany), Elisabetta Chicca (University of Groningen, Netherlands), David Kappel (Ruhr-Universität Bochum, Germany), Erika Covi (NaMLab gGmbH, Germany)

09:36 am
ID1630: A Precision-Optimized Fixed-Point Near-Memory Digital Processing Unit for Analog In-Memory Computing
Elena Ferro (IBM Research - Zürich, Switzerland), Athanasios Vasilopoulos (IBM Research - Zürich, Switzerland), Corey Lammie (IBM Research - Zürich, Switzerland), Manuel Le Gallo (IBM Research - Zürich, Switzerland), Luca Benini (Integrated Systems Laboratory, ETH Zürich, Switzerland), Irem Boybat (IBM Research - Zürich, Switzerland), Abu Sebastian (IBM Research - Zürich, Switzerland)

09:54 am
ID1742: Mismatch Calibration Strategy for Query-Driven AER Read-Out in a Memristor-CMOS Neuromorphic Chip
Luis Camuñas-Mesa (IMSE-CNM, CSIC & Universidad de Sevilla, Spain), Teresa Serrano-Gotarredona (IMSE-CNM, CSIC & Universidad de Sevilla, Spain), Bernabé Linares-Barranco (IMSE-CNM, CSIC & Universidad de Sevilla, Spain)

9:00 am – 10:30 am
C1L-12 Smart 6G Wireless Baseband: Design & Implementations
TRACK 14: SPECIAL SESSION

Venue: Virgo 2
ORAL
Session Chair(s): Chuan Zhang (Southeast University, China), Suwen Song (Sun Yat-sen University)

09:00 am
ID1124: A Scalable RISC-V Vector Processor Enabling Efficient Multi-Precision DNN Inference
Chuanning Wang (Nanjing University, China), Chao Fang (Nanjing University, China), Xiao Wu (Nanjing University, China), Zhongfeng Wang (Nanjing University, China), Jun Lin (Nanjing University, China)

09:18 am
ID2102: **HSViT: A Hardware and Software Collaborative Design for Vision Transformer via Multi-Level Compression**
Hongrui Song (Nanjing University, China), Liang Xu (Sun Yat-sen University, China), Ya Wang (Hong Kong University of Science and Technology, China), Xiao Wu (Nanjing University, China), Meiqi Wang (Sun Yat-sen University, China), Zhongfeng Wang (Nanjing University, China)

09:36 am
ID2273: **A Hardware Efficient Matrix Multiplications Scheme with Dynamic Precisions and Dimensions for Massive MIMO Systems**
Qiuyu Cheng (University of Electronic Science and Technology of China, China), Yakun Zhou (University of Electronic Science and Technology of China, China), Chentao Liang (University of Electronic Science and Technology of China, China), Zuofeng Zhang (ZTE Corporation, China), Jienan Chen (University of Electronic Science and Technology of China, China)

09:54 am
ID2307: **Code Length Compatible Belief Propagation Polar Decoder Based on Folding and Unfolding**
Muhao Li (Southeast University, China), Huizheng Wang (Southeast University, China), Yifei Shen (Southeast University, China), Xiaosi Tan (Southeast University, China), Chuan Zhang (Southeast University, China)

9:00 am – 10:30 am
C1L-13 Efficient Processing of Large Language Models at the Edge
TRACK 14: SPECIAL SESSION

Venue: Virgo 3
ORAL
Session Chair(s): Hao Zhang (Ocean University of China), Seok-Bum Ko (University of Saskatchewan)

09:00 am
ID2301: **Energy Efficient FPGA-Based Binary Transformer Accelerator for Edge Devices**
Congpeng Du (Ocean University of China, China), Seokbum Ko (University of Saskatchewan, Canada), Hao Zhang (Ocean University of China, China)

09:18 am
ID1252: **BETA: Binarized Energy-Efficient Transformer Accelerator at the Edge**
Yuhao Ji (Nanjing University, China), Chao Fang (Nanjing University, China), Zhongfeng Wang (Nanjing University, China)

09:36 am
ID1311: **DP-FFN: Block-Based Dynamic Pooling for Accelerating Feed-Forward Layers in Transformers**
Jie Tang (University of Science and Technology of China, China), Shuai Wang (University of Science and Technology of China, China), Song Chen (University of Science and Technology of China, China), Yi Kang (University of Science and Technology of China, China)

09:54 am
ID2532: **Optimized Transformer Models: ℓ 'BERT with CNN-Like Pruning and Quantization**
Muhammad Hamis Haider (University of Saskatchewan, Canada), Stephany Valarezo-Plaza (University of Saskatchewan, Canada), Sayed Muhsin (University of Saskatchewan, Canada), Hao Zhang (Ocean University of China, China), Seokbum Ko (University of Saskatchewan, Canada)

10:12 am
ID1356: Most Significant One-Driven Shifting Dynamic Efficient Multipliers for Large Language Models
Bin Gong (Nanjing University of Aeronautics and Astronautics, China), Ke Chen (Nanjing University of Aeronautics and Astronautics, China), Pengfei Huang (Nanjing University of Aeronautics and Astronautics, China), Bi Wu (Nanjing University of Aeronautics and Astronautics, China), Weiqiang Liu (Nanjing University of Aeronautics and Astronautics, China)

10:30 am – 11:00 am
Coffee Break
NETWORKING

10:30 am – 12:30 pm
C2P-14 Analog Techniques III
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Robert Sobot (University of Western Ontario)

ID1259: An Energy Efficient Delay Element with Self-Shutoff Logic and Delay Extension
Can Liang (Peking University, China), Zeyu Cai (Peking University, China)

ID1670: CMOS Implementation of Low-Frequency Pattern Generator for Electrochemical Sensing
Madhukar Gosula (Indian Institute of Technology Kharagpur, India), Ashis Maity (Indian Institute of Technology Kharagpur, India)

ID2344: Reinforcement-Learning-Based Foggy-Aware Optimal Placement Method for Analog and Mixed-Signal Circuits
Mirvala Sadrafshari (Memorial University of Newfoundland, Canada), Octavia Dobre (Memorial University of Newfoundland, Canada), Lihong Zhang (Memorial University of Newfoundland, Canada)

ID2592: A 1.35-ppm/°C Temperature Coefficient,86-dB PSR Voltage Reference with 1-mA Load Driving Capability
Haiyang Guo (Southeast University, China), Zhongyuan Fang (Southeast University, China), Haonan Fan (Southeast University, China), Shen Xu (Southeast University, China), Xueyong Zhang (Southeast University, China), Weifeng Sun (Southeast University, China)

ID2395: A 3rd-Order Noise Shaped Multistage Open-Loop Current Controlled Oscillator-Based ADC with Non-Linearity Compensation
Nordin Zbida Fernandez (Universidad Carlos III de Madrid, Spain), Susana Paton (Universidad Carlos III de Madrid, Spain), Eric Gutierrez (Universidad Carlos III de Madrid, Spain)

10:30 am – 12:30 pm
C2P-15 Analog Techniques IV
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Sohmyung Ha (New York Univeristy)

ID1266: A Transient Response Improved Digital LDO with an Approximate CEAG Analog-to-Frequency Domain Converter
Fanyang Li (Fuzhou University, China), Tao Yin (中科院半导体所, China), Faxiang Wang (Fuzhou University, China), Zhanpeng Yuan (Fuzhou University, China)

ID1904: Overcoming Impedance-Mismatch Induced Offsets in Background Bond Wire Defect Detection
Niklas Klefe (Robert Bosch GmbH & Ulm University, Germany), Rudolf Ritter (Robert Bosch GmbH, Germany), Mahdi Rajabzadeh (Bosch Sensortec, Germany), Thomas Mayer (Robert Bosch GmbH, Germany), Maurits Ortmanns (Universität Ulm, Germany)

ID1889: Modeling and Validation of Offset Cancellation for Hybrid Photonic-Electronic Transimpedance Amplifier Using All-Electronic Circuits
Jared Marchant (Brigham Young University, United States), Christian Carver (Brigham Young University, United States), Austin Barlow (Brigham Young University, United States), Benjamin Fisher (Brigham Young University, United States), John Serafini (Oak Ridge National Laboratory, United States), Nicholas Peters (Oak Ridge National Laboratory, United States), Ryan Camacho (Brigham Young University, United States), Shiuh-Hua Wood Chiang (Brigham Young University, United States)

ID2425: A mmw Low-Noise Sub-Sampling Phase-Locked Loop with a Non-Pulsed Charge Pump, Frequency Calibration and a Compact Ultra-High-Q Resonator
Patrick Kurth (Technische Universität Berlin, Germany), Philipp Scholz (Technische Universität Berlin, Germany), Philipp Nickel (Technische Universität Berlin, Germany), Urs Hecht (Technische Universität Berlin, Germany), Enne Wittenhagen (Technische Universität Berlin, Germany), Kai Misselwitz (Technische Universität Berlin, Germany), Friedel Gerfers (Technische Universität Berlin, Germany)

10:30 am – 12:30 pm
C2P-16 Electronic Design Automation & Physical Design II
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Yuhang Zhang (Shanghai Jiao Tong University)

ID1221: Machine Learning for SRAM Stability Analysis
Jihene Bouhlila (Intel Deutschland GmbH Munich & Universität zu Lübeck, Germany), Felix Last (Intel Deutschland GmbH, Germany), Rainer Buchty (Universität zu Lübeck, Germany), Mladen Berekovic (Universität zu Lübeck, Germany), Saleh Mulhem (Universität zu Lübeck, Germany)

ID1245: Net Topology Exploration and Tuning for Mitigating Congestion in Global Routing
Hwapyong Kim (Seoul National University, Korea), Taewhan Kim (Seoul National University, Korea)

ID1589: Sub-10nm Standard Cell Library Design Methodology for On-Grid Pin Accesses
Rung-Bin Lin (Yuan Ze University, Taiwan), Pei-Sheng Lu (Yuan Ze University, Taiwan)

ID1651: BCA Channel Routing to Minimize Wirelength for Generalized Channel Problem
Zezhong Wang (Tokyo Institute of Technology, Japan), Masayuki Shimoda (Tokyo Institute of Technology, Japan), Atsushi Takahashi (Tokyo Institute of Technology, Japan)

ID1923: Parallel AIG Refactoring via Conflict Breaking

Ye Cai (Shenzhen University, China), Zonglin Yang (Shenzhen University, China), Liwei Ni (PengCheng Laboratory, China), Junfeng Liu (Beihang University, China), Biwei Xie (Institute of Computing Technology, Chinese Academy of Sciences, Peng Cheng Laboratory, China), Xingquan Li (PengCheng Laboratory, China)

10:30 am – 12:30 pm
C2P-17 Electronic Design Automation & Physical Design III
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Kwen-Siong Chong (Zero-Error Systems)

ID1552: Effective Resource Model and Cost Scheme for Maze Routing in 3D Global Routing
Zirui Li (Beijing University of Posts and Telecommunications, China), Jianwang Zhai (Beijing University of Posts and Telecommunications, China), Zixuan Li (Beijing University of Posts and Telecommunications, China), Zhongdong Qi (Xidian University, China), Kang Zhao (Beijing University of Posts and Telecommunications, China)

ID1767: Design Automation for Charge Recovery Logic
Yilmaz Ege Gonul (Drexel University, United States), Leo Filippini (Drexel University, United States), Junghoon Oh (Japan Advanced Institute of Science and Technology, Japan), Ragh Kuttappa (Drexel University, United States), Scott Lerner (Drexel University, United States), Mineo Kaneko (Japan Advanced Institute of Science and Technology, Japan), Baris Taskin (Drexel University, United States)

ID1780: Redefining Clock Network Construction: The Nested Flex Paradigm for Enhanced PPA Dynamics
Lakshmi Sarvaani Pallapu (Indian Institute of Technology Tirupati, India), Subba Ramkumar Reddy Annapalli (Intel Technology India Pvt. Ltd., India), Vikramkumar Pudi (Indian Institute of Technology Tirupati, India)

ID2079: FS2K: A Forksheet FET Technology Library and a Study of VLSI Prediction for 2nm and Beyond
Yunjeong Shin (Kyungpook National University, Korea), Daehyeok Park (Kyungpook National University, Korea), Dohun Koh (Kyungpook National University, Korea), Dongryul Heo (Kyungpook National University, Korea), Jieun Park (Kyungpook National University, Korea), Hyundong Lee (Kyungpook National University, Korea), Jongbeom Kim (Kyungpook National University, Korea), Hyunsoo Lee (Kyungpook National University, Korea), Taigon Song (Kyungpook National University, Korea)

ID2394: A Rule-Based High Efficient Obstacle-Avoiding RSMT Algorithm for VLSI Routing
Junhao Guo (Sun Yat-sen University, China), Hongxin Kong (Advanced Micro Devices, Inc., United States), Lang Feng (Sun Yat-sen University, China)

10:30 am – 12:30 pm
C2P-18 Power Converters & Driver Circuits
TRACK 4: POWER AND ENERGY CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Yanhan Zeng (Guangzhou University), Tsung-Heng Tsai (National Yang Ming Chiao Tung University)

ID1013: [Three-Phase Motor Driver with Overcurrent Protection Function]
Xiaowei Zhang (Lanzhou University, China), Fangcong Wang (Lanzhou University, China), Dezhi Xing (Chengdu Huanyuxin Technology Co.,Ltd., China), Longxiang Zhu (Gansu Construction Investment (Holdings) Group Corporation Equipment Manufacturing Co., Ltd., China)

ID1071: [A 10-MHz 5-V On-Chip 6-Layer Multi-Level Digital Transformer Using T18HVG2 Process]
Oliver Jose (National Sun Yat-sen University & Batangas State University, Taiwan), Yun-Che Chang (National Sun Yat-sen University, Taiwan), Venkata Kolakaluri (National Sun Yat-sen University, India), Celso Co (Batangas State University, Philippines), Ming-Chi Chou (National Sun Yat-sen University, Taiwan), Chua-Chin Wang (National Sun Yat-sen University, Taiwan)

ID1682: [Modeling and Prediction of Common-Mode Electromagnetic Interference for GaN-Based LLC Resonant Converters]
Chuang Bi (University of Electronic Science and Technology of China, China), Siyong Luo (University of Electronic Science and Technology of China, China), Heyang Shan (University of Electronic Science and Technology of China, China), Lin Cheng (State Grid Shaanxi Electric Power Research Institute, China)

ID2214: [A GaN Driver with Almost Constant dv/dt During Miller Plateau for V-I Overlap Loss Reduction]
Yunzhe Yang (University of Macau, Macau), Qiujin Chen (University of Macau, Macau), Zaitian Yang (University of Macau, Macau), Sijun Du (Delft University of Technology, Netherlands), Mo Huang (University of Macau, Macau)

ID1711: [A GaN-Based Gate Driver with Adaptive Charge Sharing Bootstrap Technique to Improve the Conduction Loss]
Tsung-Wen Sun (National Chung Cheng University, Taiwan), Yung-Tang Hsu (National Chung Cheng University, Taiwan), Tsung-Heng Tsai (National Yang Ming Chiao Tung University, Taiwan), Chia-Chan Chang (National Chung Cheng University, Taiwan)

10:30 am – 12:30 pm
C2P-19 Wireless Communications II
TRACK 3: COMMUNICATIONS CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Wael Badawy (the International Centre for Arbitration, Egypt), Maire O'Neill (Queen's University Belfast)

ID1015: [On the Design of Reflecting Intelligent Surfaces for Multi-User NOMA Communication Networks]
Javad Shabanpour (Aalto University, Finland), Konstantin Simovski (Aalto University, Finland)

ID1474: [Channel Estimation and Equalization Design with SNR Decision Based Universal Threshold for Sub-THz Single Carrier Baseband Receiver]
Feng Ju Liao (National Yang Ming Chiao Tung University, Taiwan), Chung Lun Tu (National Yang Ming Chiao Tung University, Taiwan), Shyh Jye Jou (National Yang Ming Chiao Tung University, Taiwan)

ID1479: [Online Self-Adaptive Estimation and Compensation Design for DC Voltage Offset, Frequency-Independent, and Frequency-Dependent IQ Mismatch in Sub-THz Digital Baseband Transceiver]

Chia Jung Lee (National Yang Ming Chiao Tung University, Taiwan), Chung Lun Tu (National Yang Ming Chiao Tung University, Taiwan), Shyh Jye Jou (National Yang Ming Chiao Tung University, Taiwan)

ID1804: **Analysis of Signal Transmission Through Time-Varying Inductively Coupled Links**
Nagendra Krishnapura (Indian Institute of Technology Madras, India)

ID1477: **A 128 Gb/s LDPC Decoder Using Partial Syndrome-Based Dynamic Decoding Scheme for Terahertz Wireless Multi-Media Networks**
Tsung Han Wu (National Yang Ming Chiao Tung University, Taiwan), Ching Liang Yeh (National Yang Ming Chiao Tung University, Taiwan), Yi Shan Huang (National Yang Ming Chiao Tung University, Taiwan), Shyh Jye Jou (National Yang Ming Chiao Tung University, Taiwan)

ID1202: **A 1536-Element Ku-Band Dual-Polarized Transmit Phased Array for SATCOM Application**
Sicheng Sun (University of Electronic Science and Technology of China, China), Yijiu Zhao (University of Electronic Science and Technology of China, China), Yanze Zheng (University of Electronic Science and Technology of China, China), Naixin Zhou (University of Electronic Science and Technology of China, China), Yongling Ban (University of Electronic Science and Technology of China, China)

ID1707: **Dynamic Control of Reconfigurable Intelligent Surfaces: An IC-Based MOS Varactor Approach**
Loukas Petrou (University of Cyprus, Cyprus), Marco A. Antoniades (Toronto Metropolitan University, Canada), Julius Georgiou (University of Cyprus, Cyprus)

10:30 am – 12:30 pm
C2P-20 Machine Learning & Signal Processing for Biomedical Systems II
TRACK 6: BIOMEDICAL CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Chris Lee (National Cheng Kung University, Taiwan)

ID1170: **ADHD Classification with Robust Biomarker Detection Using Knowledge Distillation**
Yibin Tang (Hohai University, China), Linxiang Cui (Hohai University, China), Xiaotong Wang (Hohai University, China), Min Li (Hohai University, China), Ying Chen (Changzhou University, China), Yuan Gao (Hohai University, China)

ID1432: **Epilepsy Detection with Personal Identification Based on Regularized O-Minus Decomposition**
Da Shen (University of Electronic Science and Technology of China, China), Zhongrong Wang (University of Electronic Science and Technology of China, China), Fei He (University of Electronic Science and Technology of China, China), Zhijie Sun (University of Electronic Science and Technology of China, China), Ce Zhu (University of Electronic Science and Technology of China, China), Yipeng Liu (University of Electronic Science and Technology of China, China)

ID1485: **On-Chip Data Compression Techniques for High-Density Implantable Neural Recording**
Shantanu Baliyan (Indian Institute of Technology Bombay, India), Anshul Thakur (Indian Institute of Technology Bombay, India), Laxmeesha Somappa (Indian Institute of Technology Bombay, India)

ID2056: **A Real-Time Machine Learning Module for Motion Artifact Detection in fNIRS**
Renas Ercan (University of Cambridge, United Kingdom), Yunjia Xia (University College London, United Kingdom), Yunyi Zhao (University College London, United Kingdom), Rui Loureiro

(University College London, United Kingdom), Shufan Yang (Edinburgh Napier University, United Kingdom), Hubin Zhao (University College London, United Kingdom)

ID2478: **PSCS: A Physiological Sound Compression System Based on Compressive Sensing with Self-Adaptive Compression Ratio and Optimized DCT**
Changyan Chen (Shanghai Jiao Tong University, China), Rui Pan (Shanghai Jiao Tong University, China), Huajie Huang (Shanghai Jiao Tong University, China), Qing Zhang (Shanghai Jiao Tong University, China), Xuya Jiang (Jiangnan University, China), Yuhang Zhang (Shanghai Jiao Tong University, China), Jian Zhao (Shanghai Jiao Tong University, China), Yongfu Li (Shanghai Jiao Tong University, China)

10:30 am – 12:30 pm
C2P-21 Neuromorphic Systems IV
TRACK 8: NEURAL NETWORKS AND NEUROMORPHIC ENGINEERING

Venue: Leo 2+3+4
POSTER
Session Chair(s): Chang Gao (TU Delft)

ID1964: **Integrating a Hippocampus Memory Model Into a Neuromorphic Robotic-Arm for Trajectory Navigation**
Daniel Casanueva-Morato (Universidad de Sevilla, Spain), Pablo Lopez-Osorio (Universidad de Cadiz, Spain), Enrique Piñero-Fuentes (Universidad de Sevilla, Spain), Juan Pedro Dominguez-Morales (Universidad de Sevilla, Spain), Fernando Perez-Peña (Universidad de Cadiz, Spain), Alejandro Linares-Barranco (Universidad de Sevilla, Spain)

ID2141: **Two-Step Classification Neuron Circuits for Low-Power and High-Integration SNN Systems**
Da-Hyeon Youn (Dongguk University, Korea), Gyu Won Kam (Dongguk University, Korea), Minkyu Song (Dongguk University, Korea), Soo Youn Kim (Dongguk University, Korea)

ID2236: **Enhancing Memory Capacity of Reservoir Computing with Delayed Input and Efficient Hardware Implementation with Shift Registers**
Soshi Hirayae (Kyushu Institute of Technology, Japan), Kanta Yoshioka (Kyushu Institute of Technology, Japan), Atsuki Yokota (Kyushu Institute of Technology, Japan), Ichiro Kawashima (Kyushu Institute of Technology, Japan), Yuichiro Tanaka (Research Center for Neuromorphic AI Hardware, Japan), Yuichi Katori (Future University Hakodate, Japan), Osamu Nomura (Kyushu Institute of Technology, Japan), Takashi Morie (Kyushu Institute of Technology, Japan), Hakaru Tamukoh (Kyushu Institute of Technology, Japan)

ID2290: **Hybrid Event-Frame Neural Spike Detector for Neuromorphic Implantable BMI**
Vivek Mohan (Nanyang Technological University, Singapore), Wee Peng Tay (Nanyang Technological University, Singapore), Arindam Basu (City University of Hong Kong, Hong Kong)

ID2349: **On-Chip Spike Encoder to Program a Memristor-Based Synaptic Array**
Sk Hasibul Alam (University of Tennessee, United States), Hritom Das (University of Tennessee, United States), Garrett S. Rose (University of Tennessee, United States)

10:30 am – 12:30 pm
C2P-22 Image/Video Quality Assessment & Enhancement
TRACK 10: DIGITAL SIGNAL PROCESSING

Venue: Leo 2+3+4
POSTER

Session Chair(s): Guangtao Zhai (Shanghai Jiao Tong University)

ID1158: **FS-BAND: A Frequency-Sensitive Banding Detector**
Zijian Chen (Shanghai Jiao Tong University, China), Wei Sun (Shanghai Jiao Tong University, China), Zicheng Zhang (Shanghai Jiao Tong University, China), Ru Huang (East China University of Science and Technology, China), Fangfang Lu (Shanghai University of Electric Power, China), Xiongkuo Min (Shanghai Jiao Tong University, China), Guangtao Zhai (Shanghai Jiao Tong University, China), Wenjun Zhang (Shanghai Jiao Tong University, China)

ID1389: **PAPS-OVQA: Projection-Aware Patch Sampling for Omnidirectional Video Quality Assessment**
Chunyi Li (Shanghai Jiao Tong University, China), Zicheng Zhang (Shanghai Jiao Tong University, China), Haoning Wu (Nanyang Technological University, Singapore), Kaiwei Zhang (Shanghai Jiao Tong University, China), Lei Bai (Shanghai AI Laboratory, China), Xiaohong Liu (Shanghai Jiao Tong University, China), Guangtao Zhai (Shanghai Jiao Tong University, China), Weisi Lin (Nanyang Technological University, Singapore)

ID1409: **Multidimensional Similarity Fusion for Speech Quality Assessment**
Fan Huang (Shanghai Jiao Tong University, China), Xiongkuo Min (Shanghai Jiao Tong University, China), Yuqin Cao (Shanghai Jiao Tong University, China), Xiaoping Zhang (Toronto Metropolitan University, Canada), Guangtao Zhai (Shanghai Jiao Tong University, China)

ID1473: **Blind Quality Assessment of Panoramic Images Based on Multiple Viewport Sequences**
Xuelin Liu (Jiangxi University of Finance and Economics, China), Jiebin Yan (Jiangxi University of Finance and Economics, China), Zheng Wan (Jiangxi University of Finance and Economics, China), Yuming Fang (Nanyang Technological University & Jiangxi University of Finance and Economics, China), Hantao Liu (Cardiff University, United Kingdom)

ID1143: **DSA-QoE: Quality of Experience Evaluation for Streaming Video Based on Dual-Stage Attention**
Ziheng Jia (Shanghai Jiao Tong University, China), Xiongkuo Min (Shanghai Jiao Tong University, China), Guangtao Zhai (Shanghai Jiao Tong University, China)

ID1967: **PrefIQA: Human Preference Learning for AI-Generated Image Quality Assessment**
Hengjian Gao (Shanghai Jiao Tong University, China), Kaiwei Zhang (Shanghai Jiao Tong University, China), Wei Sun (Shanghai Jiao Tong University, China), Chunyi Li (Shanghai Jiao Tong University, China), Huiyu Duan (Shanghai Jiao Tong University, China), Xiaohong Liu (Shanghai Jiao Tong University, China), Xiongkuo Min (Shanghai Jiao Tong University, China), Guangtao Zhai (Shanghai Jiao Tong University, China)

10:30 am – 12:30 pm
C2P-23 Live Demo III
TRACK 15: LIVE DEMO

Venue: Leo 2+3+4
POSTER
Session Chair(s): Chao Wang (Huazhong University of Science and Technology), Deruo Cheng (Nanyang Technological University)

ID1265: **Live Demonstration: A 1920×1080 129fps 4.3pJ/Pixel Stereo-Matching Processor for Low-Power Applications**
Zhuoyu Chen (Southern University of Science and Technology, China), Shengming Zhou (Southern University of Science and Technology, China), Pingcheng Dong (Hong Kong University of Science

and Technology & Southern University of Science and Technology, China), Ke Li (Southern University of Science and Technology, China), Wenyue Zhang (Southern University of Science and Technology, China), Fengwei An (Southern University of Science and Technology, China), Lei Chen (Southern University of Science and Technology, China)

ID1454: **Live Demonstration: A Video Denoising Co-Processor with Non-Local Means Algorithm for FHD 30fps Image Sensor**
Ruoheng Yao (Southern University of Science and Technology, China), Shengming Zhou (Southern University of Science and Technology, China), Zhiyue Gao (Southern University of Science and Technology, China), Yangyi Zhang (Southern University of Science and Technology, China), Yiwei Luo (Southern University of Science and Technology, China), Lei Chen (Southern University of Science and Technology, China), Fengwei An (Southern University of Science and Technology, China)

ID1497: **Live Demonstration: Real-Time Audio and Visual Inference on the RAMAN TinyML Accelerator**
Adithya Krishna (Western Sydney University, Australia), Ashwin Rajesh (Indian Institute of Science, India), Hitesh Pavan Oleti (Indian Institute of Science, India), Anand Chauhan (Indian Institute of Science, India), Shankaranarayanan H (Indian Institute of Science, India), André van Schaik (Western Sydney University, Australia), Mahesh Mehendale (Indian Institute of Science, India), Chetan Singh Thakur (Indian Institute of Science, India)

ID2257: **Live Demonstration: A Reconfigurable, Energy-Efficient and High-Frame-Rate EKF-SLAM Accelerator Based SoC Design for Autonomous Mobile Robot Applications**
Dingcheng Jiang (Huazhong University of Science and Technology, China), Bingqiang Liu (Huazhong University of Science and Technology, China), Jipeng Wang (Huazhong University of Science and Technology, China), Ao Hu (Huazhong University of Science and Technology, China), Yequan Zhao (University of California, Santa Barbara & Huazhong University of Science and Technology, China), Minjie Bao (Harbin Institute of Technology, China), Zhendong Fan (Harbin Institute of Technology, China), Zixuan Shen (Huazhong University of Science and Technology, China), Ke Wang (Harbin Institute of Technology, China), Chao Wang (Huazhong University of Science and Technology, China)

ID2450: **Live Demonstration: A High-Frame-Rate and Energy-Efficient SIFT Feature Extraction**
Accelerator Based SoC Design for AMR Applications
Zhenhui Duan (Huazhong University of Science and Technology, China), Bingqiang Liu (Huazhong University of Science and Technology, China), Zehua Yin (Huazhong University of Science and Technology, China), Jipeng Wang (Huazhong University of Science and Technology, China), Zixuan Shen (Huazhong University of Science and Technology, China), Xupeng Zhang (Huazhong University of Science and Technology, China), Zaisheng He (Amicro Semiconductor Company Ltd., China), Chao Wang (Huazhong University of Science and Technology, China)

ID2554: **Live Demonstration: W3M Wearable Weight and Walk Monitoring System**
Asim Arif (Khalifa University, U.A.E.), Adedayo Adegbile (Khalifa University, U.A.E.), Qiraat Khan (Khalifa University, U.A.E.), Hamda Memon (Khalifa University, U.A.E.), Ibrahim Elfadel (Khalifa University, U.A.E.)

10:30 am – 12:30 pm
C2P-24 Multimedia Applications & Visual Representation
TRACK 12: MULTIMEDIA SYSTEMS AND APPLICATIONS

Venue: Leo 2+3+4
POSTER

Session Chair(s): Guangtao Zhai (Shanghai Jiao Tong University)

ID1090: **Calculating Color Differences of Images via Siamese Neural Network**
Yixuan Gao (Shanghai Jiao Tong University, China), Xiongkuo Min (Shanghai Jiao Tong University, China), Xiaohong Liu (Shanghai Jiao Tong University, China), Lei Sun (Tencent, China), Yonglin Luo (Tencent, China), Zuowei Cao (Tencent, China), Guangtao Zhai (Shanghai Jiao Tong University, China)

ID1230: **Tangible User Interface Everywhere Based on Imperceptible Structured Light**
Jiawen Xue (Tsinghua University, China), Xuguang Zhang (Tsinghua University, China), Guolin Li (Tsinghua University, China), Xiang Xie (Tsinghua University, China)

ID1835: **System Integration of Xilinx DPU and HDMI for Real-Time Inference in PYNQ Environment with Image Enhancement**
Jonathan Sanderson (Tennessee Tech University, United States), Syed Rafay Hasan (Tennessee Tech University, United States)

ID1360: **Enhancing Cross-Modal Understanding for Audio Visual Scene-Aware Dialog Through Contrastive Learning**
Feifei Xu (Shanghai University of Electric Power, China), Wang Zhou (Shanghai University of Electric Power, China), Guangzhen Li (Shanghai University of Electric Power, China), Zheng Zhong (Shanghai University of Electric Power, China), Yingchen Zhou (Shanghai University of Electric Power, China)

10:30 am – 12:30 pm
C2P-25 Integrated Biomedical & Biosensing Circuits & Systems
TRACK 6: BIOMEDICAL CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Pantelis Georgiou (Imperial College London)

ID1112: **A Low-Power Non-Uniform Third-Derivative-Based Sampling Technique for ECG Applications**
Bahareh Shirmohammadi (University of British Columbia, Canada), Reza Molavi (University of British Columbia, Canada), Shahriar Mirabbasi (University of British Columbia, Canada)

ID1440: **Rapid Diagnostics for Colorectal Cancer Using Lab-on-Chip Technology with Machine Learning**
Calista Adele Yapeter (Imperial College London, United Kingdom), Costanza Gulli (Imperial College London, United Kingdom), Katerina-Theresa Mantikas (Imperial College London, United Kingdom), Francis Lali (Imperial College London, United Kingdom), Nicolas Moser (Imperial College London, United Kingdom), Constantinos Simillis (Imperial College London, United Kingdom), Melpomeni Kalofonou (Imperial College London, United Kingdom), Pantelis Georgiou (Imperial College London, United Kingdom)

ID1980: **A Miniaturized Chip-Based ODNP Platform**
Qing Yang (University of Stuttgart, Germany), Hadi Lotfi (University of Stuttgart, Germany), Frederik Dreyer (University of Stuttgart, Germany), Michal Kern (University of Stuttgart, Germany), Jens Anders (University of Stuttgart, Germany)

ID2008: **Simultaneous Quantification of Multiple Drugs by Machine Learning on Electrochemical Sensors**

Tatsunori Matsumoto (École Polytechnique Fédérale de Lausanne; Shibaura Institute of Technology, Switzerland), Lin Du (École Polytechnique Fédérale de Lausanne, Switzerland), Yann Thoma (HES-SO University of Applied Sciences and Arts Western Switzerland, Switzerland), Sandro Carrara (École Polytechnique Fédérale de Lausanne, Switzerland)

ID2186: A Low-Power Spike Detector Using In-Memory Computing for Event-Based Neural Frontend
Ye Ke (City University of Hong Kong, Hong Kong), Arindam Basu (City University of Hong Kong, Hong Kong)

11:00 am – 12:30 pm
C3L-01 Analog Techniques I
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Aquarius 1
ORAL
Session Chair(s): Edoardo Bonizzoni (University of Pavia), Liheng Lou (University of Science and Technology of China)

11:00 am
ID1831: Block Configuration Algorithms for a Reconfigurable Analog Array
Ziyi Chen (Drexel University, United States), Ioannis Savidis (Drexel University, United States)

11:18 am
ID2032: Configurable and Intelligent Switched CMOS Current Driver Powering Arrays of Electrothermal Actuators for MEMS Switches
Allan Riboullet (École de Technologie Supérieure ÉTS, Canada), Frédéric Nabki (École de Technologie Supérieure ÉTS, Canada), Yves Blaquière (École de Technologie Supérieure ÉTS, Canada), Glenn Cowan (Concordia University, Canada)

11:36 am
ID2185: Implementation of Floating Charged Memristor Emulator Utilizing DVCCTA
Nidhee Bhuwal (International Institute of Information Technology, Naya Raipur, India), Manoj Kumar Majumder (International Institute of Information Technology, Naya Raipur, India), Deepika Gupta (International Institute of Information Technology, Naya Raipur, India)

11:54 am
ID1541: A Low Power Programmable Switch Supply Dynamic Comparator
Madhan Venkatesh (Microelectronic Circuits Centre Ireland, University College Cork, Ireland), Gerardo Molina Salgado (Microelectronic Circuits Centre Ireland, University College Cork, Ireland), Kevin McCarthy (University College Cork, Ireland), Ivan O'Connell (Analog Devices S.r.l., Ireland)

12:12 pm
ID2055: A 19 fJ/op, Low-Offset StrongARM Latch Comparator for Low-Power High-Speed Applications
Abdullah Alshehri (King Abdullah University of Science and Technology, Saudi Arabia), Khaled Salama (King Abdullah University of Science and Technology, Saudi Arabia), Hossein Fariborzi (King Abdullah University of Science and Technology, Saudi Arabia)

11:00 am – 12:30 pm
C3L-02 Voltage Reference Circuits
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Aquarius 2

ORAL
Session Chair(s): Xinsheng Wang (Harbin Institute of Technology), Yanhan Zeng (Guangzhou University)

11:00 am
ID1549: A Dual Mode All NMOS 7-T Temperature Sensor and Voltage Reference for Biomedical Applications
Dipesh Monga (Aalto University, Finland), Kari Halonen (Aalto University, Finland)

11:18 am
ID1697: Analysis and Design of Chopperless 7 ppm/°C Bandgap Voltage Reference
Rakesh Kumar Palani (Indian Institute of Technology Delhi, India)

11:36 am
ID2502: A 2.3-ppm/℃ High-Order Compensated Bandgap Reference with Low-Cost Current Trimming
Yuze Weng (Shanghai Jiao Tong University, China), Jinlei Pan (Shanghai Jiao Tong University, China), Yang Zhao (Shanghai Jiao Tong University, China), Junmin Jiang (Southern University of Science and Technology, China), Liang Qi (Shanghai Jiao Tong University, China)

11:54 am
ID1442: A 0.7-V and 10-nA CMOS-Only Voltage Reference with 1-mA Load Driving Capability Based on Gate-Voltage Compensation Loop
Yanshen Luo (Guangzhou University, China), Wenjian Huang (Guangzhou University, China), Yuying Huang (Guangzhou University, China), Yongfu Li (Shanghai Jiao Tong University, China), Yanhan Zeng (Guangzhou University, China)

12:12 pm
ID1460: Design and Analysis of a Family of pW-Level Sub-1V CMOS VRGs by Stacking a Current-Source Transistor and a Resistive-Load Transistor
Tong Zhang (Shanghai Jiao Tong University, China), Dingguo Zhang (Shanghai Jiao Tong University, China), Jing Jin (Shanghai Jiao Tong University, China), Patrick Mercier (University of California, San Diego, United States), Hui Wang (Shanghai Jiao Tong University, China)

11:00 am – 12:30 pm
C3L-03 Programmable & Reconfigurable Array Architectures
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Aquarius 3
ORAL
Session Chair(s): Fakhrul Zaman Rokhani (University Putra Malaysia), Malgorzata Chrzanowska-Jeske (Portland State University)

11:00 am
ID1300: Accelerating Frequency-Domain Convolutional Neural Networks Inference Using FPGAs
Yi Chen (Guangdong University of Technology, China), Bosheng Liu (Guangdong University of Technology, China), Yongqi Xu (Guangdong University of Technology, China), Jigang Wu (Guangdong University of Technology, China), Xiaoming Chen (Chinese Academy of Sciences, China), Peng Liu (Guangdong University of Technology, China), Qingguo Zhou (Lanzhou University, China), Yinhe Han (Chinese Academy of Sciences, China)

11:18 am
ID1893: A 119.64 GOPs/W FPGA-Based ResNet50 Mixed-Precision Accelerator Using the Dynamic DSP Packing (TCAS-II paper)
Yaozhong Ou (University of Macau, Macau), Wei-Han Yu (State Key Laboratory of Analog and Mixed-Signal VLSI, AMSV, University of Macau, Macau), Ka-Fai Un (University of Macau, Macau), Chi-Hang Chan (State Key Laboratory of Analog and Mixed-Signal VLSI, AMSV, University of Macau, Macau), Yan Zhu (University of Macau, Macau)

11:36 am
ID2089: A 420 GOPS/W CGRA with a Configurable MAC and Dynamic Truncation
Yi Sheng Chong (Institute of Microelectronics, Agency for Science, Technology and Research, Singapore), Rakshith Harish (National University of Singapore, Singapore), Rajesh Panicker (National University of Singapore, Singapore), Vishnu Paramasivam Nambiar (Institute of Microelectronics, Agency for Science, Technology and Research, Singapore), Anh Tuan Do (Institute of Microelectronics, Agency for Science, Technology and Research, Singapore)

11:54 am
ID2365: Dynamically Configurable FIR Filters Based on Serial MACs and Systolic Arrays
Ruan Bo (Shanghai University, China), Limin Jiang (Shanghai University, China), Shan Cao (Shanghai University, China), Zhiyuan Jiang (Shanghai University, China)

12:12 pm
ID1225: Hybrid Multi-Tile Vector Systolic Architecture for Accelerating Convolution on FPGAs
Jay Shah (International Institute of Information Technology Bangalore, India), Nanditha Rao (International Institute of Information Technology Bangalore, India)

11:00 am – 12:30 pm
C3L-04 Ultra-low Power Circuits & Systems
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Aquarius 4
ORAL
Session Chair(s): Kwen-Siong Chong (Zero-Error Systems), Mladen Berekovic (Universität zu Lübeck)

11:00 am
ID1732: Constrained Sorter Design Using Zero-One Principle
Sangil Han (Pohang University of Science and Technology & Samsung Electronics, Korea), Jaehee Kim (Pohang University of Science and Technology, Korea), Dongyun Kam (Pohang University of Science and Technology, Korea), Byeong Yong Kong (Kongju National University, Korea), Mijung Kim (Pohang University of Science and Technology, Korea), Young-Seok Kim (Pohang University of Science and Technology, Korea), Youngjoo Lee (Pohang University of Science and Technology, Korea)

11:18 am
ID1127: Design of CNFET-Based Ternary Conditional Sum Adders Using Binary Carry Propagation
Chetan Kumar Vudadha (Birla Institute of Technology and Science, Pilani, India)

11:36 am
ID1354: Dynamically Adaptive Accumulator for In-Sensor ANN Hardware Accelerators

Andrea Fasolino (University of Salerno, Italy), Paola Vitolo (University of Salerno, Italy), Rosalba Liguori (University of Salerno, Italy), Luigi Di Benedetto (University of Salerno, Italy), Alfredo Rubino (University of Salerno, Italy), Gian Domenico Licciardo (University of Salerno, Italy)

11:54 am
ID1653: Cost-Efficient SIMD ASIP Architecture for Mobile Touchscreen Controllers
Eunbin Park (Pohang University of Science and Technology, Korea), Myungjun Jin (HIDEEP, Korea), Youngjoo Lee (Pohang University of Science and Technology, Korea)

12:12 pm
ID1911: Low-Power Encoder and Compressor Design for Approximate Radix-8 Booth Multiplier
Jiwoo Kim (Pohang University of Science and Technology, Korea), Gunho Park (Pohang University of Science and Technology, Korea), Youngjoo Lee (Pohang University of Science and Technology, Korea)

11:00 am – 12:30 pm
C3L-05 Advanced CMOS, Cryogenics and 3D Integration
TRACK 5: BEYOND CMOS: NANOELECTRONICS AND HYBRID SYSTEMS INTEGRATION

Venue: Gemini 1
ORAL
Session Chair(s): Sorin Cotofana (TU Delft), Georgios Sirakoulis (Democritus University of Thrace)

11:00 am
ID1481: Improved RF Performance with Buried Power Rail and Contact Over Active Gate in Nanosheet FETs
Hao-Chi Chiu (National Taiwan University, Taiwan), Vita Pi-Ho Hu (National Taiwan University, Taiwan)

11:18 am
ID2018: The Optimization of Aging-Aware 8T SRAM for FPGA Configuration Memory
Yifei Li (ShanghaiTech University, China), Yuxin Zhou (ShanghaiTech University, China), Yuhao Shu (ShanghaiTech University, China), Hongyu Chen (Fudan University, China), Yajun Ha (ShanghaiTech University, China)

11:36 am
ID1153: A 0.01-to-2.6-GHz Two-Fold Current Reuse Noise-Canceling LNA for Quantum Applications (TCAS-II paper)
Mahesh Kumar Chaubey (National Tsing Hua University, Taiwan), Chih-Cheng Lin (National Tsing Hua University, Taiwan), Yin-Cheng Chang (Taiwan Semiconductor Research Institute, National Applied Research Laboratories, Taiwan), Po-Chang Wu (Taiwan Semiconductor Research Institute, National Applied Research Laboratories, Taiwan), Hann-Huei Tsai (Taiwan Semiconductor Research Institute, National Applied Research Laboratories, Taiwan), Shawn S.H. Hsu (National Tsing Hua University, Taiwan)

11:54 am
ID1888: A 4-7 GHz Broadband Cryogenic GaAs mHEMT LNA with a Flatness Gain Variation of ±1.2 dB
Che Hao Li (Industrial Technology Research Institute, Taiwan), Tzu Han Su (National Yang Ming Chiao Tung University, Taiwan), Chien-Nan Kuo (National Yang Ming Chiao Tung University, Taiwan)

12:12 pm
ID1231: Monolithic 3D Transposable 3T Embedded DRAM with Back-end-of-Line Oxide Channel Transistor
Jungyoun Kwak (Georgia Institute of Technology, United States), Gihun Choe (Georgia Institute of Technology, United States), Junmo Lee (Georgia Institute of Technology, United States), Shimeng Yu (Georgia Institute of Technology, United States)

11:00 am – 12:30 pm
C3L-06 Dynamic & Event-Driven Vision Sensors
TRACK 7: SENSORY CIRCUITS AND SYSTEMS

Venue: Gemini 2
ORAL
Session Chair(s): Chiara Bartolozzi (Istituto Italiano di Tecnologia, Genova, Italy), Xiaojin Zhao (Shenzhen University)

11:00 am
ID1058: A Dual-Mode CMOS Image Sensor Based on in-Pixel Frame Differencing
Xu Ren (Peking University, China), Liqiao Liu (Peking University, China), Yandong He (Peking University, China), Gang Du (Peking University, China)

11:18 am
ID1956: An Event-Driven High-Speed Imaging and Trace Detection ROIC for Cryogenic Infrared FPAs
Mingzhong He (Peking University, China), Yufei Ai (Peking University, China), Wengao Lu (Peking University, China), Yi Zhuo (Peking University, China), Qingjiang Xia (Peking University, China), Runkun Zhu (Peking University, China), Yacong Zhang (Peking University, China), Zhongjian Chen (Peking University, China)

11:36 am
ID1989: A Discrete Approach to Dynamic Vision with Single-Photon Detectors
Ruben Gomez-Merchan (University of Seville, Spain), Juan Antonio Leñero-Bardallo (IMSE-CNM, CSIC & Universidad de Sevilla, Spain), Pablo Fernández-Peramo (IMSE-CNM, CSIC & Universidad de Sevilla, Spain), Ángel Rodríguez-Vázquez (University of Seville, Spain)

11:54 am
ID1119: An End-to-End Deep-Learning-Based Indirect Time-of-Flight Image Signal Processor
Annan Xiong (Hong Kong University of Science and Technology; AI Chip Center for Emerging Smart System, Hong Kong), Yuzhong Jiao (Hong Kong University of Science and Technology; AI Chip Center for Emerging Smart System, Hong Kong), Xuejiao Liu (Hong Kong University of Science and Technology; AI Chip Center for Emerging Smart System, Hong Kong), Manto Yung (Hong Kong University of Science and Technology; AI Chip Center for Emerging Smart System, Hong Kong), Xianghong Hu (Hong Kong University of Science and Technology; AI Chip Center for Emerging Smart System, Hong Kong), Luhong Liang (Hong Kong University of Science and Technology; AI Chip Center for Emerging Smart System, Hong Kong), Jie Yuan (Hong Kong University of Science and Technology; AI Chip Center for Emerging Smart System, Hong Kong), Mansun Chan (Hong Kong University of Science and Technology; AI Chip Center for Emerging Smart System, Hong Kong)

12:12 pm
ID2329: tinyRadar: LSTM-Based Real-Time Multi-Target Human Activity Recognition for Edge Computing

Satyapreet Singh Yadav (Indian Institute of Science, India), Shreyansh Anand (Indian Institute of Science, India), Adithya M D (Indian Institute of Science, India), Nikitha Sai Dasari (Indian Institute of Science, India), Chetan Singh Thakur (Indian Institute of Science, India)

11:00 am – 12:30 pm
C3L-07 Biomedical Circuits & Systems II
TRACK 6: BIOMEDICAL CIRCUITS AND SYSTEMS

Venue: Pisces 1
ORAL
Session Chair(s): Jingna Mao (Chinese Academy of Sciences, China), Zhiping Lin (Nanyang Technological University)

11:00 am
ID1961: Precise and Tunable TΩ Pseudo-Resistors Based on Process-Independent pA-Level Current Sources and DACs
Jiahe Li (ShanghaiTech University, China), Ruoyu Chu (ShanghaiTech University, China), Ziqi Li (ShanghaiTech University, China), Hongming Lyu (ShanghaiTech University, China)

11:18 am
ID1873: A High-Throughput Impedance Measurement IC with Baseline-Canceling Peak Detector
Asra Malik (National University of Sciences & Technology, Pakistan), Soon-Jae Kweon (Catholic University of Korea, Korea), Karam Ellahi (National University of Sciences & Technology, Pakistan), Muhammad Abrar Akram (New York University Abu Dhabi, U.A.E.), Song-I Cheon (Korea Advanced Institute of Science and Technology, Korea), Yoontae Jung (Korea Advanced Institute of Science and Technology, Korea), Minkyu Je (Korea Advanced Institute of Science and Technology, Korea), Hammad M. Cheema (National University of Sciences & Technology, Pakistan), Sohmyung Ha (New York University Abu Dhabi, U.A.E.)

11:36 am
ID2469: Adaptive Digitally-Controlled Active Rectifier-Based Receiver for Bioimplants
Sayan Sarkar (Hong Kong University of Science and Technology, Hong Kong), Yuan Yao (Hong Kong University of Science and Technology, Hong Kong), Wing-Hung Ki (Hong Kong University of Science and Technology, Hong Kong), Chi-Ying Tsui (Hong Kong University of Science and Technology, Hong Kong)

11:54 am
ID2528: A Current DAC Based Current Generator with Fourth-Order Current-Mode Filter for Electrical Impedance Tomography
Jiayang Li (University College London, United Kingdom), Yu Wu (University College London, United Kingdom), Dai Jiang (University College London, United Kingdom), Richard Bayford (Middlesex University, United Kingdom), Andreas Demosthenous (University College London, United Kingdom)

12:12 pm
ID1816: A Versatile 8-Channel High Voltage Stimulator for Comprehensive Neural Stimulation
Kuan-Ting Lin (National Yang Ming Chiao Tung University, Taiwan), Ming-Dou Ker (National Yang Ming Chiao Tung University, Taiwan)

11:00 am – 12:30 pm
C3L-08 Neuromorphic Systems II
TRACK 8: NEURAL NETWORKS AND NEUROMORPHIC ENGINEERING

Venue: Pisces 2

ORAL
Session Chair(s): Yifei Shen (École Polytechnique Fédérale de Lausanne), Chetan Singh Thakur (India Institute of Science)

11:00 am
ID1637: TNNGen: Automated Design of Neuromorphic Sensory Processing Units for Time-Series Clustering (TCAS-II paper)
Prabhu Vellaisamy (Carnegie Mellon University, United States), Harideep Nair (Carnegie Mellon University, United States), Vamsikrishna Ratnakaram (Carnegie Mellon University, United States), Dhruv Gupta (Carnegie Mellon University, United States), John Paul Shen (Carnegie Mellon University, United States)

11:18 am
ID2473: A Near-Eye DVS-Based End-to-End Eye Tracking Processor for AR/VR Applications
Shihang Tan (Fudan University, China), Jiayu Huang (Fudan University, China), Quanshu Yan (Fudan University, China), Lirong Zheng (Fudan University, China), Zhuo Zou (Fudan University, China)

11:36 am
ID1244: Optoelectronic Computing Evaluation and Deployment Platform Based on a 256-Mac Silicon Photonic Chip
Likai Li (Nanjing University, China), Yichuan Bai (Nanjing University, China), Shengping Liu (United Microelectronics Center, China), Yang Zhao (United Microelectronics Center, China), Sunan He (Nanjing University, China), Yaqing Li (Nanjing University, China), Li Du (Nanjing University, China), Yuan Du (Nanjing University, China)

11:54 am
ID1320: A Lightweight and Accurate CORDIC-Based Digital Implementation of the Hindmarsh-Rose Neuron
Alexander J. Leigh (University of Windsor, Canada), Moslem Heidarpur (University of Windsor, Canada), Mitra Mirhassani (University of Windsor, Canada)

12:12 pm
ID1695: Low Quantization Error Readout Circuit with Fully Charge-Domain Calculation for Computation-in-Memory Deep Neural Network
Ao Shi (Peking University, China), Yizhou Zhang (Peking University, China), Lixia Han (Peking University, China), Zheng Zhou (Peking University, China), Yiyang Chen (Peking University, China), Lifeng Liu (Peking University, China), Linxiao Shen (Peking University, China), Peng Huang (Peking University, China), Xiaoyan Liu (Peking University, China), Jinfeng Kang (Peking University, China)

11:00 am – 12:30 pm
C3L-09 Filter Design, Implementation & Application
TRACK 10: DIGITAL SIGNAL PROCESSING

Venue: Pisces 3
ORAL
Session Chair(s): Gordana Jovanovic Dolecek (National Institute of Astrophysics, Optics and Electronics, Mexico), Mrityunjoy Chakrabor (Indian Institute of Technology (IIT), Kharagpur)

11:00 am
ID2274: Minimax Design of M-D Interpolated FIR Filters Using Convex-Concave Procedure
Pathmapirian Nanthakumar (University of Queensland, Australia), Chamira U. S. Edussooriya (University of Moratuwa, Sri Lanka), Chamith Wijenayake (University of Queensland, Australia), Arjuna Madanayake (Florida International University, United States)

11:18 am
ID2336: Parallelized Hardware Acceleration of Automatic Differentiating Wave Digital Filters
Lech Kolonko (University of Wuppertal, Germany), Jörg Velten (University of Wuppertal, Germany), Anton Kummert (University of Wuppertal, Germany)

11:36 am
ID1027: A New Design of All-Pass IIR Filters Based Two-Channel Quadrature Mirror Filter Bank
Shengzhe Gao (Hangzhou Dianzi University, China), Shi Li (Hangzhou Dianzi University, China), Xiangzhen Li (Hangzhou Dianzi University, China), Hao Wang (Hangzhou Dianzi University, China), Zhihua Jian (Hangzhou Dianzi University, China), Cheng Zha (Zhejiang Technical Institute of Economics, China)

11:54 am
ID1736: A Proportionate Type Block-Oriented Functional Link Adaptive Filter for Sparse Nonlinear Systems
Pavankumar Ganjimala (Indian Institute of Technology Palakkad, India), Subrahmanyam Mula (Indian Institute of Technology Palakkad, India)

12:12 pm
ID1621: Advanced Equalization: List DFE Combined with LLR-Based Error Propagation Mitigation
Mücahit Furkan Yıldız (ADHOC Teknoloji A.Ş., Turkey), Ertuğrul Kolağasıoğlu (ADHOC Teknoloji A.Ş., Turkey), Ahmet Baran Kaygusuz (ADHOC Teknoloji A.Ş., Turkey), Halil Cirit (Meta Inc., United States)

11:00 am – 12:30 pm
C3L-10 Brain Computer Interface: Hardware & Circuit Design
TRACK 14: SPECIAL SESSION

Venue: Pisces 4
ORAL
Session Chair(s): Minkyu Je (KAIST, Korea), Yoshifumi Nishio (Tokushima University, Japan)
11:00 am
ID2270: A Novel Design of Ergodic Sequential Logic Integrated Cochlear Model for Reproduction of Nonlinear Compression Characteristics of Mammalian Cochlea and Efficient Implementation
Koki Sone (Hosei University, Japan), Hiroyuki Torikai (Hosei University, Japan)

11:18 am
ID2177: An Intracortical Wireless Bidirectional Brain-Computer Interface with High Data Density
Linghui Kong (Institute of Automation, Chinese Academy of Sciences, China), Zhiwei Zhang (Institute of Automation, Chinese Academy of Sciences, China), Shan Yu (Institute of Automation, Chinese Academy of Sciences, China), Jingna Mao (Institute of Automation, Chinese Academy of Sciences, China)

11:36 am
ID1298: A High Efficiency, Low EMI Non-Inverting Buck-Boost Converter in Wireless Power and Data Transfer System for Brain Computer Interface
Xiangsheng Xu (Tsinghua University, China), Qihang Zhang (Tsinghua University, China), Tengfei Ma (Tsinghua University, China), Songping Mai (Tsinghua University, China)

11:54 am
ID2275: High-Precision Noise-Shaping SAR ADC Using KT/C Noise Cancellation Within CIFF Path for Brain-Machine Interface Application
Fukun Su (Tsinghua University, China), Mingqi Sun (Tsinghua University, China), Chao Wang (Tsinghua University, China), Xian Tang (Tsinghua University, China)

12:12 pm
ID2205: Algorithm-Hardware Co-Design for Wearable BCIs: An Evolution from Linear Algebra to Transformers
Sunyoung Park (EWHA Womans University, Korea), Wooseok Byun (SAPEON Korea Inc., Korea), Minkyu Je (Korea Advanced Institute of Science and Technology, Korea), Ji-Hoon Kim (EWHA Womans University, Korea)

11:00 am – 12:30 pm
C3L-11 Improving the Accuracy & Reliability of Analog-Based In-Memory Computing Systems II
TRACK 14: SPECIAL SESSION

Venue: Virgo 1
ORAL
Session Chair(s): Corey Lammie (IBM Research - Zurich), Jason K. Eshraghian (University of California, Santa Cruz)

11:00 am
ID1849: Optimal Data Distribution in FeFET-Based Computing-in-Memory Macros
Yonguk Sim (Hanyang University, Korea), Choongseok Song (Hanyang University, Korea), Eun Chan Park (Hanyang University, Korea), Jongwook Jeon (Sungkyunkwan University, Korea), Daewoong Kwon (Hanyang University, Korea), Doo Seok Jeong (Hanyang University, Korea)

11:18 am
ID2445: Bio-Plausible Learning-on-Chip with Selector-Less Memristive Crossbars
Jeong-Hoon Kim (University of California, San Diego, United States), Soumil Jain (University of California, San Diego, United States), Gopabandhu Hota (University of California, San Diego, United States), Jaeseoung Park (University of California, San Diego, United States), Ashwani Kumar (University of California, San Diego, United States), Duygu Kuzum (University of California, San Diego, United States), Gert Cauwenberghs (University of California, San Diego, United States)

11:36 am
ID1794: Novel SRAM Based Temporary Memory for PVT Variation Tolerant Analog In-Memory Computing
Sivakumar Elangovan (Indian Institute of Technology Bombay, India), Porus Vangala (Indian Institute of Technology Bombay, India), Yeshwanth Sunnapu (Indian Institute of Technology Bombay, India), Khalid Shaikh (Indian Institute of Technology Bombay, India), Udayan Ganguly (Indian Institute of Technology Bombay, India), Maryam Shojaei Baghini (Indian Institute of Technology Bombay, India)

11:54 am
ID2134: In-Memory Transformer Self-Attention Mechanism Using Passive Memristor Crossbar
Jack Cai (University of Toronto, Canada), Muhammad Ahsan Kaleem (University of Toronto, Canada), Roman Genov (University of Toronto, Canada), Mostafa Rahimi Azghadi (James Cook University, Australia), Amirali Amirsoleimani (York University, Canada)

11:00 am – 12:30 pm
C3L-12 Recent Progress in Analysis & Estimation of Bifurcation Phenomena
TRACK 14: SPECIAL SESSION

Venue: Virgo 2
ORAL
Session Chair(s): Masaharu Adachi (Tokyo Denki University), Yoshitaka Itoh (Hokkaido University of Science)

11:00 am
ID1414: **Neimark-Sacker Bifurcation in DC-DC Converter with Photovoltaic Module**
Hiroyuki Asahara (Okayama University of Science, Japan), Takuji Kousaka (Chukyo University, Japan)

11:18 am
ID1878: **Predicting a Critical Transition from Time-Series Datasets Generated by LTspice Using a Parameter Space Estimation**
Yoshitaka Itoh (Hokkaido University of Science, Japan)

11:36 am
ID1894: **Bifurcation Phenomena Observed from Two-Variable Spiking Neuron Integrated Circuit**
Takemori Orima (Tohoku University, Japan), Yoshihiko Horio (Tohoku University, Japan), Satoshi Moriya (Tohoku University, Japan), Shigeo Sato (Tohoku University, Japan)

11:00 am – 12:30 pm
C3L-13 Ultra-Low-Power ICs Enabling Sensor Nodes Without Batteries
TRACK 14: SPECIAL SESSION

Venue: Virgo 3
ORAL
Session Chair(s): Volkan Kursun (Bilkent University), Orazio Aiello (University of Genoa)

11:00 am
ID1308: **A 15-nA Quiescent Current Capacitor-Less LDO for Sub-1V µW-Powered Fully-Harvested Systems**
Marco Privitera (Università degli studi di Catania, Italy), Andrea Ballo (Università degli studi di Catania, Italy), Alfio Dario Grasso (Università degli studi di Catania, Italy), Massimo Alioto (National University of Singapore, Singapore)

11:18 am
ID1368: **A Feedback Self-Adaptive Body Biasing-Based RF-DC Rectifier for Highly-Sensitive RF Energy Harvesting**
Jun Yin (University of Virginia, United States), Elisa Pantoja (University of Virginia, United States), Yimin Gao (University of Virginia, United States), Mircea Stan (University of Virginia, United States)

11:36 am
ID2208: **A 0.4 V 180 nm CMOS Sub-µW Ultra-Compact and Low-Effort Design PWM-Based ADC**
Guido Di Patrizio Stanchieri (University of L'Aquila, Italy), Orazio Aiello (Università di Genova, Italy), Andrea De Marcellis (University of L'Aquila, Italy)

11:54 am
ID2212: Inverter-Based Amplifier with Active Frequency Compensation and Adaptive Voltage Scaling
Luís Henrique Rodovalho (Synopsys, Inc., Portugal), Orazio Aiello (Università di Genova, Italy)

12:12 pm
ID2342: Fully Synthesizable Dynamic Voltage Comparator Across Technology Nodes and Scaled Supply Voltages
Duy-Hieu Bui (Vietnam National University, Hanoi, Vietnam), Duc-Mạnh Tran (Vietnam National University, Hanoi, Vietnam), Daniele D. Caviglia (Università di Genova, Italy), Orazio Aiello (Università di Genova, Italy)

12:30 pm – 1:30 pm
Lunch
NETWORKING

Venue: B2 Ballroom

1:30 pm – 5:00 pm
Technology for the Elderly (GeronCAS)
EMBEDDED WORKSHOP

Venue: Leo 1
Session Chair(s): Prof. Mohd Nazim Mohtar (Universiti Putra Malaysia, Malaysia)

1:30 pm – 3:00 pm
C4L-01 Photonics & mm-Wave Circuits
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Aquarius 1
ORAL
Session Chair(s): Vishal Saxena (University of Delaware), Xi Zhu (University of Technology Sydney)

1:30 pm
ID1925: A 24.3-to-44.8 GHz Reconfigurable Dual-Band T/R Front-End with an Implicit Switch-Based Antenna Interface Supporting 600MSym/s 64QAM
Junlong Gong (Tsinghua University, China), Wei Deng (Tsinghua University, China), Fuyuan Zhao (Tsinghua University, China), Haikun Jia (Tsinghua University, China), Wenjing Ye (Tsinghua University, China), Ruichen Wan (Tsinghua University, China), Baoyong Chi (Tsinghua University, China)

1:48 pm
ID1318: Bandwidth Enhancement Techniques for Large-Area VLC Receivers
Amany Kassem (University College London, United Kingdom), Izzat Darwazeh (University College London, United Kingdom)

2:06 pm
ID1117: Fast Mutual-Heating Prediction Method for Integrated Electronics and Photonics
Thomas Booij (Eindhoven University of Technology, Netherlands), Marco Fattori (Eindhoven University of Technology, Netherlands), Peter Baltus (Eindhoven University of Technology, Netherlands)

2:24 pm
ID2421: **A Wideband Linear GaN-on-SiC Power Amplifier Using Harmonic-Tuning Technique for 5G New-Radio FR2 Applications**
Yi-Fan Tsao (National Yang Ming Chiao Tung University, Taiwan), Heng-Tung Hsu (National Yang Ming Chiao Tung University, Taiwan)

1:30 pm – 3:00 pm
C4L-02 RF & mm-Wave Circuits I
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Aquarius 2
ORAL
Session Chair(s): Raafat Lababidi (ENSTA Bretagne), Yanhan Zeng (Guangzhou University)

1:30 pm
ID2465: **A 14~18 GHz Compact Double-Pole Triple-Throw Switch Based Multi-Phase Integrated 6-Bit Passive Phase Shifter**
Yang Wang (University of the Chinese Academy of Sciences, China), Chenhao Li (Institute of Microelectronics Chinese Academy of Sciences, China), Qingyang Dong (Institute of Microelectronics Chinese Academy of Sciences, China), Chunyue Bo (Institute of Microelectronics Chinese Academy of Sciences, China), Xiuhao Wu (Institute of Microelectronics Chinese Academy of Sciences, China), Ke Wei (Institute of Microelectronics Chinese Academy of Sciences, China), Xinyu Liu (Institute of Microelectronics Chinese Academy of Sciences, China), Weijun Luo (Institute of Microelectronics Chinese Academy of Sciences, China)

1:48 pm
ID1710: **High-Order Multilayer Input-Absorptive RF Filter with Wideband Quasi-Flat Group Delay and Multiple Stopband Transmission Zeros**
Li Yang (University of Alcalá, Spain), Mohamed Malki (University of Alcalá, Spain), José-María Muñoz-Ferreras (University of Alcalá, Spain), Xi Zhu (University of Technology Sydney, Australia), Roberto Gómez-García (University of Alcalá, Spain)

2:06 pm
ID1060: **A Narrowband RF Front End in 22-nm FD-SOI Featuring a Programmable Low-Noise** Amplifier with a Configurable Noise-Power Trade-Off
Marco Gonzalez (Université catholique de Louvain, Belgium), Pol Maistriaux (Université catholique de Louvain, Belgium), David Bol (Université catholique de Louvain, Belgium)

2:24 pm
ID2200: **A Millimeter-Wave Input-Reflectionless Amplifier in 45-nm SOI CMOS Technology**
Jim Darell Ang (University of Technology Sydney, Australia), Li Yang (University of Alcalá, Spain), Roberto Gómez-García (University of Alcalá, Spain), Xi Zhu (University of Technology Sydney, Australia)

2:42 pm
ID2345: **A Tunable Switched-Capacitor 2-Way Power Divider Based on N-Path Filters**
M Mahmudul Hasan Sajeeb (University of California, Santa Barbara, United States), Sandeep Reddy Kukunuru (University of California, Santa Barbara, United States), Loai G. Salem (University of California, Santa Barbara, United States)

1:30 pm – 3:00 pm
C4L-03 Hardware Security for Logic, Circuits & Architectures I
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Aquarius 3
ORAL
Session Chair(s): Chip Hong Chang (Nanyang Technological University), Ayesha Khalid (Queen's University of Belfast)

1:30 pm
ID1991: REVBiT: Reverse Engineering of Bitstream for LUT Extraction & Logic Identification
Anmol Singh Narwariya (Indian Institute of Technology Hyderabad, India), Chetan Talele (Vellore Institute of Technology, Andhra Pradesh, India), Pabitra Das (Indian Institute of Technology Hyderabad, India), Amit Acharyya (Indian Institute of Technology Hyderabad, India)

1:48 pm
ID2449: SHP-FsNTT: A Scalable and High-Performance NTT Accelerator Based on the Four-Step Algorithm
Xiaojie Chen (Sun Yat-sen University, China), Weicong Lu (Sun Yat-sen University, China), Tao Su (Sun Yat-sen University, China), Dihu Chen (Sun Yat-sen University, China)

2:06 pm
ID1194: Unified Lossless-Throughput Architecture for AES and SM4 Encryption with Changeable Keys
Zhishuo Huang (Sun Yat-sen University, China), Jia Tao (Huawei Technologies Co., Ltd., China), Haosong Zhao (Guangdong Provincial Key Laboratory IRADS, BNU-HKBU United International College, China), Donglong Chen (Guangdong Provincial Key Laboratory IRADS, BNU-HKBU United International College, China), Shuyan Zhu (Sun Yat-sen University, China), Yinjin Fu (Sun Yat-sen University, China), Nong Xiao (Sun Yat-sen University, China), Yao Liu (Sun Yat-sen University, China)

2:24 pm
ID1776: Passive Lightweight On-Chip Sensors for Power Side Channel Attack Detection
Nael Mizanur Rahman (Georgia Institute of Technology, United States), Uday Kamal (Georgia Institute of Technology, United States), Venkata Chaitanya Krishna Chekuri (Georgia Institute of Technology, United States), Arvind Singh (Georgia Institute of Technology, United States), Saibal Mukhopadhyay (Georgia Institute of Technology, United States)

2:42 pm
ID2006: Novel PUF Based on Generalized Galois Ring Oscillators with 10-15 EER and 0.53% BER
Raúl Aparicio-Téllez (Universidad de Zaragoza, Spain), Miguel Garcia-Bosque (Universidad de Zaragoza, Spain), Guillermo Díez-Señorans (Universidad de Zaragoza, Spain), Santiago Celma (Universidad de Zaragoza, Spain)

1:30 pm – 3:00 pm
C4L-04 Advanced Techniques for Digital Integrated Circuits & Systems I
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Aquarius 4
ORAL
Session Chair(s): Robert Chen-Hao Chang (National Chung Hsing University), Mircea Stan (University of Virginia)

1:30 pm
ID2087: Q-Learning Assisted LASSO-Based Thermal Sensor Placement for Thermal-Aware Multi-Core Systems

Kun-Chih Chen (National Yang Ming Chiao Tung University, Taiwan), Lei-Qi Wang (National Sun Yat-sen University, Taiwan)

1:48 pm
ID1154: A 0.8-Ps RMS Precision Period Jitter Measurement Circuit with Offset Reduction
Lin Xie (Shanghai Jiao Tong University, China), Zizheng Dong (Shanghai Jiao Tong University, China), Jialei Sun (Shanghai Jiao Tong University, China), Sai Gao (Shanghai Jiao Tong University, China), Shuaipeng Li (Shanghai Jiao Tong University, China), Naifeng Jing (Shanghai Jiao Tong University, China), Qin Wang (Shanghai Jiao Tong University, China), Jianfei Jiang (Shanghai Jiao Tong University, China)

2:06 pm
ID1423: PUF-Based Lightweight Mutual Authentication Protocol for Internet of Things (IoT) Devices
Kamal Raj (Indian Institute of Technology Mandi, India), Srinivasu Bodapati (Indian Institute of Technology Mandi, India), Anupam Chattopadhyay (Nanyang Technological University, Singapore)

2:24 pm
ID2354: Dynamic Resource Management in Reconfigurable SoC for Multi-Tenancy Support
Sohyeon Kim (EWHA Womans University, Korea), Injun Choi (Korea Advanced Institute of Science and Technology, Korea), Minkyu Je (Korea Advanced Institute of Science and Technology, Korea), Ji-Hoon Kim (EWHA Womans University, Korea)

2:42 pm
ID1537: Enabling Efficient Hardware Acceleration of Hybrid Vision Transformer (ViT) Networks at the Edge
Joren Dumoulin (Katholieke Universiteit Leuven, Belgium), Pouya Houshmand (Katholieke Universiteit Leuven, Belgium), Vikram Jain (University of California, Berkeley, United States), Marian Verhelst (Katholieke Universiteit Leuven, Belgium)

1:30 pm – 3:00 pm
C4L-05 Computing with Emergent Technologies II
TRACK 5: BEYOND CMOS: NANOELECTRONICS AND HYBRID SYSTEMS INTEGRATION

Venue: Gemini 1
ORAL
Session Chair(s): Vita Pi-Ho Hu (National Taiwan University), Sorin Cotofana (TU Delft)

1:30 pm
ID1226: Design Framework for Ising Machines with Bistable Latch-Based Spins and All-to-All Resistive Coupling
Yimin Wang (National University of Singapore, Singapore), Yunuo Cen (National University of Singapore, Singapore), Xuanyao Fong (National University of Singapore, Singapore)

1:48 pm
ID1529: Double Locally Active Memristor-Based Inductor-Free Chaotic Circuit
Qingdian Geng (Hangzhou Dianzi University, China), Yan Liang (Hangzhou Dianzi University, China), Zhenzhou Lu (Hangzhou Dianzi University, China), Herbert Ho-Ching Iu (University of Western Austrlia, Australia), Guangyi Wang (Hangzhou Dianzi University, China)

2:06 pm
ID2549: A Memristor Circuit Implementing Tunable Stochastic Distributions for Bayesian Inference and Monte Carlo Sampling

Adil Malik (Imperial College London, United Kingdom), Christos Papavassiliou (Imperial College London, United Kingdom)

2:24 pm
ID1118: A 250MΩ Input Impedance a-IGZO Front-End for Biosignal Acquisition from Non-Contact Electrodes
Kyle van Oosterhout (Eindhoven University of Technology, Netherlands), Martijn Timmermans (Eindhoven University of Technology, Netherlands), Marco Fattori (Eindhoven University of Technology, Netherlands), Eugenio Cantatore (Eindhoven University of Technology, Netherlands)

2:42 pm
ID2541: Low-Power Collision Avoidance Memristive Circuit for Swarms of Miniature Robots
Ioannis K. Chatzipaschalis (Democritus University of Thrace, Greece), Theodoros Panagiotis Chatzinikolaou (Democritus University of Thrace, Greece), Emmanouil Stavroulakis (Democritus University of Thrace, Greece), Evangelos Tsipas (Democritus University of Thrace, Greece), Iosif-Angelos Fyrigos (Democritus University of Thrace, Greece), Antonio Rubio (Universitat Politècnica de Catalunya, Spain), Georgios Ch. Sirakoulis (Democritus University of Thrace, Greece)

1:30 pm – 3:00 pm
C4L-06 Sensory Signals Processing Circuits
TRACK 7: SENSORY CIRCUITS AND SYSTEMS

Venue: Gemini 2
ORAL
Session Chair(s): Ibrahim Elfadel (Khalifa University of Science and Technology, Abu Dhabi, AUE), Paula López (Universidade de Santiago de Compostela, Spain)

1:30 pm
ID1772: A 2.56-µs Dynamic Range, 31.25-ps Resolution 2-D Vernier Digital-to-Time Converter (DTC) for Cell-Monitoring
Heng-Yu Liu (National Yang Ming Chiao Tung University, Taiwan), Lin-Hung Lai (National Yang Ming Chiao Tung University, Taiwan), Wen-Yue Lin (National Yang Ming Chiao Tung University, Taiwan), Yu-Wei Lu (National Yang Ming Chiao Tung University, Taiwan), Yi-Wei Lin (National Yang Ming Chiao Tung University, Taiwan), Chen-Yi Lee (National Yang Ming Chiao Tung University, Taiwan)

1:48 pm
ID1304: A Reconfigurable Multimodal Sensor Interface IC Based on Direct-Conversion ΔΣ Modulator Structure
Jimin Koo (Korea Advanced Institute of Science and Technology, Korea), Yoontae Jung (Korea Advanced Institute of Science and Technology, Korea), Sein Oh (Korea Advanced Institute of Science and Technology, Korea), Sunglim Han (Korea Advanced Institute of Science and Technology, Korea), Sohmyung Ha (New York University Abu Dhabi, U.A.E.), Minkyu Je (Korea Advanced Institute of Science and Technology, Korea)

2:06 pm
ID1446: A Low-Power Lock-In Amplifier Suitable for Implementation on a Programmable System On-Chip
Takahiro Fujita (Meiji University, Japan), Kazuyuki Wada (Meiji University, Japan)

2:24 pm
ID2444: Multi-Segment Stretchable Strain Sensor Using Time Domain Reflectometry
Calder Wilson (Oregon State University, United States), Matthew Johnston (Oregon State University, United States)

2:42 pm
ID1346: Backscatter Sensing with Single-Tag Path Variation Cancelling
Taotao Wu (Fudan University, China), Yuxiao Zhao (Fudan University, China), Kuanfeng Tang (Fudan University, China), Haoyu Jiang (Fudan University, China), Wentao Liu (Fudan University, China), Tuo Hu (Fudan University, China), Meng Liu (Fudan University, China), Hanyang Wang (Fudan University, China), Hao Min (Fudan University, China)

1:30 pm – 3:00 pm
C4L-07 Wearable Biomedical Circuits & Systems I
TRACK 6: BIOMEDICAL CIRCUITS AND SYSTEMS

Venue: Pisces 1
ORAL
Session Chair(s): Junchao Wang (Chongqing University), Danilo Demarchi (Politecnico di Torino)

1:30 pm
ID2065: A Peak-Detector-Based Ultra Low Power ECG ASIC for Early Detection of Cardio-Vascular Diseases
Sidharth Thomas (Indian Institute of Technology Roorkee & University of California, Los Angeles, India), Jaskirat Singh Virdi (Indian Institute of Technology Roorkee & University of California, Los Angeles, India), Anshul Verma (Indian Institute of Technology Roorkee, India), Bishnu Prasad Das (Indian Institute of Technology Roorkee, India), Kenichi Okada (Tokyo Institute of Technology, Japan), Pratap Narayan Singh (VerveSemi Microelectronics Pvt. Ltd., India)

1:48 pm
ID1535: A 1.37 µW, 1.68 µVrms ECG AFE with Embedded DC-Servo Loop, Digital Calibration Unit and Three-State Ripple Reduction Loop
Huiwen Shi (Guangzhou University, China), Yuchen Bao (Guangzhou University, China), Zihong He (Guangzhou University, China), Yongfu Li (Shanghai Jiao Tong University, China), Yanhan Zeng (Guangzhou University, China)

2:06 pm
ID2401: A Low-Power Predictive Sampling PPG Sensor
Zobair Ebrahimi (Laval University, Canada), Benoit Gosselin (Laval University, Canada)

2:24 pm
ID1717: An Adaptive Common-Mode Cancellation Biopotential Amplifier for Two-Electrode Dynamic ECG Recording
Zhong Zhang (University of Electronic Science and Technology of China, China), Zhangyuan Xie (University of Electronic Science and Technology of China, China), Qi Yu (University of Electronic Science and Technology of China, China), Kejun Wu (University of Electronic Science and Technology of China, China), Jing Li (University of Electronic Science and Technology of China, China), Ning Ning (University of Electronic Science and Technology of China, China)

2:42 pm
ID2414: EarFDA: A Lightweight and Energy-Efficient Fall Detection Accelerator for Ear-Worn Devices
Zhaodong Lv (ShanghaiTech University, China), Hao Sun (ShanghaiTech University, China), Yuhao Shu (ShanghaiTech University, China), Yajun Ha (ShanghaiTech University, China)

1:30 pm – 3:00 pm
C4L-08 Neural Memristive In-Memory Computation Systems

TRACK 8: NEURAL NETWORKS AND NEUROMORPHIC ENGINEERING

Venue: Pisces 2
ORAL
Session Chair(s): Shijun Liang (Nanjing University), Jianshi Tang (Tsinghua University)

1:30 pm
ID1219: VPU-CIM: A 130nm, 33.98 TOPS/W RRAM Based Compute-in-Memory Vector Co-Processor
Chithambara Moorthii J (Indian Institute of Technology Delhi, India), Vinay Rayapati (International Institute of Information Technology Bangalore, India), Nanditha Rao (International Institute of Information Technology Bangalore, India), Manan Suri (Indian Institute of Technology Delhi, India)

1:48 pm
ID2170: NURODE: In-Memory Crossbar Core for Hodgkin-Huxley Model ODE-Based Computations
Andy Gong (University of Toronto, Canada), Mostafa Rahimi Azghadi (James Cook University, Australia), Roman Genov (University of Toronto, Canada), Amirali Amirsoleimani (York University, Canada)

2:06 pm
ID2093: ReShare: A Resource-Efficient Weight Pattern Sharing Scheme for Memristive DNN Accelerators
Shihao Hong (Chinese University of Hong Kong, Shenzhen, China), Yeh-Ching Chung (Chinese University of Hong Kong, Shenzhen, China)

2:24 pm
ID2028: Stable Diffusion with Memristive Cellular Neural Networks
András Horváth (Pázmány Péter Catholic University, Hungary)

2:42 pm
ID1312: Memristor-Based Hardware and Algorithms for Higher-Order Hopfield Optimization Solver Outperforming Quadratic Ising Machines
Mohammad Hizzani (Forschungszentrum Jülich GmbH, Germany), Arne Heittmann (Forschungszentrum Jülich GmbH, Germany), George Hutchinson (University of California, Santa Barbara, United States), Dmitrii Dobrynin (Forschungszentrum Jülich GmbH, Germany), Thomas Van Vaerenbergh (Hewlett Packard Enterprise, Belgium), Tinish Bhattacharya (University of California, Santa Barbara, United States), Adrien Renaudineau (Université Paris-Saclay, France), Dmitri Strukov (University of California, Santa Barbara, United States), John Paul Strachan (Forschungszentrum Jülich GmbH, Germany)

1:30 pm – 3:00 pm
C4L-09 Machine Learning for Speech & Language Processing

TRACK 10: DIGITAL SIGNAL PROCESSING

Venue: Pisces 3
ORAL
Session Chair(s): Tokunbo Ogunfunmi (Santa Clara University, US)

1:30 pm
ID2118: TFA-Conformer Enhanced Network for Short Utterance Speaker Recognition
Lu Yang (South China University of Technology, China), Bangcheng Zhang (South China University of Technology, China), Junmei Yang (South China University of Technology, China), Delu Zeng (South China University of Technology, China)

1:48 pm
ID1685: An End-to-End Model with Comprehensive Attention for Monaural Speech Separation
Bangcheng Zhang (South China University of Technology, China), Lu Yang (South China University of Technology, China), Junmei Yang (South China University of Technology, China), Delu Zeng (South China University of Technology, China)

2:06 pm
ID1660: Multi-Kernel Attention Encoder for Time-Domain Speech Separation
Zengrun Liu (Shandong University, China), Diya Shi (Shandong University, China), Ying Wei (Shandong University, China)

2:24 pm
ID1545: Automatic Personality Recognition via XLNet with Refined Highway and Switching Module for Chatbot
Oscal Tzyh-Chiang Chen (National Chung Cheng University, Taiwan), Cheng-Hong Tsai (National Chung Cheng University, Taiwan), Manh-Hung Ha (Vietnam National University, Vietnam)

1:30 pm – 3:00 pm
C4L-10 Intelligent & Data Analytics to Real-Life Complex Networks & Nonlinear Systems I
TRACK 14: SPECIAL SESSION

Venue: Pisces 4
ORAL
Session Chair(s): Dong Liu (City University of Hong Kong), Yongxiang Xia (Hangzhou Dianzi University)

1:30 pm
ID1185: Fault Diagnosis for Hybrid AC/DC Power System Based on Convolutional Neural Network with Transfer Learning
Chang Sun (Hangzhou Dianzi University, China), Yifan Zuo (Hangzhou Dianzi University, China), Jinyue Lu (Hangzhou Dianzi University, China), Yongxiang Xia (Hangzhou Dianzi University, China), Haicheng Tu (Hangzhou Dianzi University, China), Chunshan Liu (Hangzhou Dianzi University, China)

1:48 pm
ID1724: Detecting Fake Deposit Attacks on Cross-Chain Bridges from a Network Perspective
Kaixin Lin (Sun Yat-sen University, China), Dan Lin (Sun Yat-sen University, China), Ziye Zheng (Sun Yat-sen University, China), Yixiang Tan (Sun Yat-sen University, China), Jiajing Wu (Sun Yat-sen University, China)

2:06 pm
ID1968: Bubble or Not: An Analysis of Ethereum ERC721 and ERC1155 Non-Fungible Token Ecosystem
Yixiang Tan (Sun Yat-sen University, China), Zhiying Wu (Sun Yat-sen University, China), Jieli Liu (Sun Yat-sen University, China), Jiajing Wu (Sun Yat-sen University, China), Ting Chen (University of Electronic Science and Technology of China, China), Kaixin Lin (Sun Yat-sen University, China)

2:24 pm
ID1979: An Emergent EV Dispatching Method to Enhance the Resilience of Power-Transportation Coupling Systems
Jie Yang (Beijing Institute of Technology, China), Xi Zhang (Beijing Institute of Technology, China), Xingtang Wu (North China Electric Power University, China)

2:42 pm
ID2237: Associative Memory Function Using Coupled Oscillators with Sparse Coupling
Kento Fukuta (Tokushima University, Japan), Yoko Uwate (Tokushima University, Japan), Yoshifumi Nishio (Tokushima University, Japan)

1:30 pm – 3:00 pm
C4L-11 Artificial Intelligence in Power & Energy Circuits & Systems I
TRACK 14: SPECIAL SESSION

Venue: Virgo 1
ORAL
Session Chair(s): Herbert Ho-Ching Lu (University of Western Australia), Junrui Liang (ShanghaiTech University)

1:30 pm
ID1370: Deterministic Policy Gradient Based Reinforcement Learning for Current Control of Hybrid Active Power Filter
Cheng Gong (University of Macau, Macau), Chio-Hong Leong (University of Macau, Macau), Chi-Seng Lam (University of Macau, Macau)

1:48 pm
ID1822: Efficient Probabilistic Optimal Power Flow Assessment Using an Adaptive Stochastic Spectral Embedding Surrogate Model
Xiaoting Wang (McGill University, Canada), Jingyu Liu (McGill University, Canada), Xiaozhe Wang (McGill University, Canada)

2:06 pm
ID1910: MetaCirc: A Meta-Learning Approach for Statistical Leakage Estimation Improvement in Digital Circuits
Nouduru Venkata Raghavendra (International Institute of Information Technology Hyderabad, India), Deepthi Amuru (International Institute of Information Technology Hyderabad, India), Zia Abbas (International Institute of Information Technology Hyderabad, India)

2:24 pm
ID2083: Machine Learning Based Design of Magnetic Coupler for Wireless Power Transfer
Wenhua Ding (South China University of Technology, China), Yufei Wang (South China University of Technology, China), Tingyu Chen (South China University of Technology, China), Mengna Luo (South China University of Technology, China), Jinpeng Lei (South China University of Technology, China), Yaofeng Liang (South China University of Technology, China), Zhicong Huang (South China University of Technology, China)

2:42 pm
ID2238: D^2 Buck Converter with Delay-Insensitive Response and Adaptive On-Time Extension During Load Transient
Linfeng Zhu (Hong Kong University of Science and Technology, Hong Kong), Wing-Hung Ki (Hong Kong University of Science and Technology, Hong Kong), Yue Zhong (Hong Kong University of Science and Technology, Hong Kong), Xiaofei Ma (Hong Kong University of Science and Technology, Hong Kong), Junmin Jiang (Southern University of Science and Technology, China)

1:30 pm – 3:00 pm
C4L-12 Emerging AI-driven Visual Computing & Multimodal Learning for Real-world Applications

TRACK 14: SPECIAL SESSION

Venue: Virgo 2
ORAL
Session Chair(s): Kejun Wu(Nanyang Technological University), Yi Wang (Hong Kong Polytechnic University)

1:30 pm
ID1293: **Multi-Scale Attentive Fusion Network for Remote Sensing Image Change Captioning**
Chen Cai (Nanyang Technological University, Singapore), Yi Wang (Hong Kong Polytechnic University, Hong Kong), Kim-Hui Yap (Nanyang Technological University, Singapore)

1:48 pm
ID1443: **Fusing EO and LiDAR for SAR Image Translation with Multi-Modal Generative Adversarial Networks**
Jiang Zhu (Nanyang Technological University, Singapore), Yuanyuan Qing (Nanyang Technological University, Singapore), Zhiping Lin (Nanyang Technological University, Singapore), Bihan Wen (Nanyang Technological University, Singapore)

2:06 pm
ID1874: **Few-Shot Class-Agnostic Counting with Occlusion Augmentation and Localization**
Yuejiao Su (Hong Kong Polytechnic University, Hong Kong), Yi Wang (Hong Kong Polytechnic University, Hong Kong), Lei Yao (Hong Kong Polytechnic University, Hong Kong), Lap-Pui Chau (Hong Kong Polytechnic University, Hong Kong)

2:24 pm
ID1567: **TPARN: A Network for Enhancing Synthetic Video Quality After 3D-HEVC Encoding**
Ziyi Cao (Chongqing Normal University, China), Tiansong Li (Chongqing Normal University, China), Shaoguo Cui (Chongqing Normal University, China), Kejun Wu (Nanyang Technological University, Singapore), Yan Chen (Chongqing Normal University, China), Longwei Zhong (Chongqing Normal University, China), Hongkui Wang (Hangzhou Dianzi University, China), Li Yu (Huazhong University of Science and Technology, China)

2:42 pm
ID2107: **Complex Motion Planning for Quadruped Robots Using Large Language Models**
Xiang Zhang (South China University of Technology, China), Run He (South China University of Technology, China), Kai Tong (South China University of Technology, China), Shuquan Man (South China University of Technology, China), Jingyu Tong (South China University of Technology, China), Haodong Li (South China University of Technology, China), Huiping Zhuang (South China University of Technology, China)

1:30 pm – 3:00 pm
C4L-13 Theory & Applications of Memristor Devices, Circuits, & Systems for Bio-Inspired Electronics I
TRACK 14: SPECIAL SESSION

Venue: Virgo 3
ORAL
Session Chair(s): Alex James (Digital University Kerala), Alon Ascoli (Technische Universität Dresden)

1:30 pm
ID1912: **Amorphous Silicon Single Photon Avalanche Diode Integrated with Memristor for Short Term Memory Based Rapid Passive Quenching**

Zidu Li (Siegen University, Germany), Phil David Börner (Siegen University, Germany), Soumya Shatakshi Panda (Siegen University, Germany), Maurice Müller (Siegen University, Germany), Andreas Bablich (Siegen University, Germany), Peter Haring Bolívar (Siegen University, Germany), Bhaskar Choubey (Siegen University, Germany)

1:48 pm
ID2542: Variability Tolerance Analysis of Memristive Wave Cellular Automata
Theodoros Panagiotis Chatzinikolaou (Democritus University of Thrace, Greece), Ioannis K. Chatzipaschalis (Democritus University of Thrace, Greece), Emmanouil Stavroulakis (Democritus University of Thrace, Greece), Evangelos Tsipas (Democritus University of Thrace, Greece), Iosif-Angelos Fyrigos (Democritus University of Thrace, Greece), Antonio Rubio (Universitat Politècnica de Catalunya, Spain), Georgios Ch. Sirakoulis (Democritus University of Thrace, Greece)

2:06 pm
ID2477: Hybrid Digital/Analog Memristor-Based Computing Architecture for Sparse Deep Learning Acceleration
Qilin Zheng (Duke University, United States), Shiyu Li (Duke University, United States), Yitu Wang (Duke University, United States), Ziru Li (Duke University, United States), Yiran Chen (Duke University, United States), Hai Li (Duke University, United States)

2:24 pm
ID2533: Design Space Exploration of Memristor-Based Delay Cells for Time-Domain Neuromorphic Computing
Hagar Hendy (Rochester Institute of Technology, United States), Karsten Bergthold (Rochester Institute of Technology, United States), Tejasvi Das (Rochester Institute of Technology, United States), Cory Merkel (Rochester Institute of Technology, United States)

2:42 pm
ID2076: Exploring the Global Dynamics of Networks Trained Through Equilibrium Propagation
Gianluca Zoppo (Politecnico di Torino, Italy), Fernando Corinto (Politecnico di Torino, Italy), Marco Gilli (Politecnico di Torino, Italy)

3:00 pm – 3:30 pm
Coffee Break
NETWORKING

3:00 pm – 5:00 pm
C5P-14 Interface Circuits
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Sohmyung Ha (New York Univeristy)

ID1092: A 1.41µW Motion Sensing Front-End for Passive Infrared Sensors
Siyu Wang (University of Michigan, United States), David Wentzloff (University of Michigan, United States)

ID1614: A 5.80 ns, 22.77 fJ, Energy Efficient Level Shifter Using Auto Switch Logic
Can Liang (Peking University, China), Zeyu Cai (Peking University, China)

ID1779: Ultrahigh-G Accelerometer Readout IC with Adaptive Gain Path for Shock Resilience

Song-I Cheon (Korea Advanced Institute of Science and Technology, Korea), Seonghyun Park (Korea Advanced Institute of Science and Technology, Korea), Haidam Choi (Korea Advanced Institute of Science and Technology, Korea), Yebin Choi (Korea Advanced Institute of Science and Technology, Korea), Minho Seok (Korea Advanced Institute of Science and Technology, Korea), Young-Ho Cho (Korea Advanced Institute of Science and Technology, Korea), Sohmyung Ha (New York University Abu Dhabi, U.A.E.), Minkyu Je (Korea Advanced Institute of Science and Technology, Korea)

ID1820: **A Novel 2.7 pJ/bit, Low Supply, Power Efficient, Wide-Range 2.5±6 Gb/s Transmitter for 4-Channel High-Speed Serial Transmit Port (HSSTP) in 28nm FD-SOI Technology**
Sameer Vashishtha (STMicroelectronics, India), Prashant Kumar Singh (STMicroelectronics, India), Mohd Rizvi (STMicroelectronics, India), Paras Garg (STMicroelectronics, India)

3:00 pm – 5:00 pm
C5P-15 RF & mm-Wave Circuits II
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Raafat Lababidi (ENSTA Bretagne)

ID1250: **A Compact 25-32 GHz High IMRR Double Quadrature CMOS Transmitter for 5G Applications**
Anik Batabyal (Indian Institute of Technology Bombay, India), Rajesh Zele (Indian Institute of Technology Bombay, India)

ID1538: **An Inductor-Less, Cost-Effective On-Chip CMOS VNA for Bio-Molecule Detection**
Bhartipudi Sahishnavi (International Institute of Information Technology Hyderabad, India), Samriddhi Agarwal (International Institute of Information Technology Hyderabad, India), Shameer Basha Yerragudi (International Institute of Information Technology Hyderabad, India), Naveen Dasari (International Institute of Information Technology Hyderabad, India), Andleeb Zahra (International Institute of Information Technology Hyderabad, India), Prabhakar Bhimalapuram (International Institute of Information Technology Hyderabad, India), Syed Azeemuddin (International Institute of Information Technology Hyderabad, India), Zia Abbas (International Institute of Information Technology Hyderabad, India)

ID1781: **A CMOS Wideband Linear Low-Noise Amplifier Using Dual Capacitor-Cross-Coupled Configurations**
Benqing Guo (Chengdu University of Information Technology, China), Jun Chen (Huawei Technologies Co., Ltd., China)

ID2175: **A 0.12mm² K/Ka Band RX Front-End in 40-nm CMOS with Inductor-Less LO Generators**
Haoyu Bai (Peking University, China), Dong Wang (Peking University, China), Sihao Zhang (Peking University, China), Han Huang (Peking University, China), Junhua Liu (Peking University, China), Huailin Liao (Peking University, China)

ID2574: **A Tunable FDD Duplexer Using Electrical Balance with N-Path Filters**
H S Trinath Tammisetti (Indian Institute of Technology Hyderabad, India), Nikhil Malgundkar (Indian Institute of Technology Hyderabad, India), Abhishek Kumar (Indian Institute of Technology Hyderabad, India)

3:00 pm – 5:00 pm
C5P-16 Digital Integrated Circuits & Systems
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Tony Tae-Hyoung Kim (Nanyang Technological University)

ID1431: Track Assignment Using Gradient Indication and Simulated Annealing
Yuanrui Qi (Southwest University of Science and Technology, China), Zejun Gan (Southwest University of Science and Technology, China), Jinghao Ding (Southwest University of Science and Technology, China), Zhaoqi Fu (Southwest University of Science and Technology, China), Mengshi Gong (Southwest University of Science and Technology, China), Wenxin Yu (Southwest University of Science and Technology, China)

ID1441: Hierarchical Placement Algorithm for Analog Circuit with Polygonal Modules
Mengzhe Han (Beihang University, China), Xiaotao Jia (Beihang University, China), Zihao Zhao (Beihang University, China), Yingchun Hu (Beihang University, China)

ID1622: Conure: Surrogate-Based Artwork Generator for RFCMOS Integrated Inductors
Habibur Rahman (University of Oslo, Norway), Adrian Llop Recha (University of Oslo, Norway), Stefano Fasciani (University of Oslo, Norway), Pål Gunnar Hogganvik (University of Oslo, Norway), Kristian Gjertsen Kjelgård (University of Oslo, Norway), Dag Trygve Wisland (University of Oslo, Norway)

ID1096: A 16.41 TOPS/W CNN Accelerator with Event-Based Layer Fusion for Real-Time Inference
Jiawei Wang (Peking University, China), Li Lun (Peking University, China), Zhenhui Dai (Peking University, China), Yuanyuan Jiang (Peking University, China), Xiaoxin Cui (Peking University, China)

ID1523: Enhancing the PE Utilization for Multi-Precision Systolic Array via Optimizing Computation Latency
Jing Feng (National University of Defense Technology, China), Mei Wen (National University of Defense Technology, China), Xin Ju (National University of Defense Technology, China), Junzhong Shen (National University of Defense Technology, China), Yang Guo (National University of Defense Technology, China)

ID1764: Efficient FFT-Based CNN Acceleration with Intra-Patch Parallelization and Flex-Stationary Dataflow
Shine Parekkadan Sunny (Indian Institute of Technology Palakkad, India), Satyajit Das (Indian Institute of Technology Palakkad, India)

ID1824: Rapid Emulation of Approximate DNN Accelerators
Amirreza Farahbakhsh (Sharif University of Technology, Iran), Seyedmehdi Hosseini (Sharif University of Technology, Iran), Sajjad Kachuee (Sharif University of Technology, Iran), Mohammad Sharifkhani (Sharif University of Technology, Iran)

ID1100: Redefining Trust: Assessing Reliability of Machine Learning Algorithms in Intrusion Detection Systems
Hossein Sayadi (California State University, Long Beach, United States), Zhangying He (California State University, Long Beach, United States), Tahereh Miari (Claremont Graduate University, United States), Mehrdad Aliasgari (California State University, Long Beach, United States)

ID1571: zeroShare: Constructing a Cache Covert Channel Without Memory Sharing

Zheliang Xu (University of the Chinese Academy of Sciences, China), Shan Li (University of the Chinese Academy of Sciences, China), Haihua Shen (University of Chinese Academy of Sciences, China)

ID1577: **A Light-Weight and Tamper-Resistant AES Implementation by FPGAs**
Yui Koyanagi (Fukuoka University, Japan), Tomoaki Ukezono (Fukuoka University, Japan), Toshinori Sato (Fukuoka University, Japan)

ID1405: **MEIN: A Multicast-Efficient Interconnect Network for Multi-Chiplet DNN Accelerators**
Hao Chen (Shanghai Jiao Tong University, China), Xuyan Wang (Shanghai Jiao Tong University, China), Jinming Zhang (Shanghai Jiao Tong University, China), Xiao Han (Shanghai Jiao Tong University, China), Siqi Cai (Shanghai Jiao Tong University, China), Yaoyao Ye (Shanghai Jiao Tong University, China), Guanghui He (Shanghai Jiao Tong University, China)

ID1224: **A Hardware Instruction Generation Mechanism for Energy-Efficient Computational Memories**
Léo De La Fuente (Université Grenoble Alpes, CEA List, France), Jean-Frédéric Christmann (Université Grenoble Alpes, CEA List, France), Manuel Pezzin (Université Grenoble Alpes, CEA List, France), Matthias Remars (Université Grenoble Alpes, CEA List, France), Olivier Sentieys (Inria centre at Rennes University, France)

ID1813: **SRAM-Based Hybrid Analog Compute-in-Memory Architecture to Enhance the Signal Margin**
Dinesh Kushwaha (Indian Institute of Technology Roorkee, India), Rajiv Joshi (IBM T. J. Watson Research Center, United States), Sudeb Dasgupta (Indian Institute of Technology Roorkee, India), Anand Bulusu (Indian Institute of Technology Roorkee, India)

ID2009: **Design of High-Density Iso-Stable Asymmetric Memory Cell with Upto 10X Reduced Leakage**
Ajay Shroti (Indraprastha Institute of Information Technology, Delhi, India), Anuj Grover (Indraprastha Institute of Information Technology, Delhi, India)

ID1915: **A Novel DA-Based Parallel Architecture for Inner-Product of Variable Vectors**
Anil Kali (University of Hyderabad, India), Samrat L. Sabat (University of Hyderabad, India), Pramod Kumar Meher (C. V. Raman Global University, India)

3:00 pm – 5:00 pm
C5P-17 Advanced Memory & Computing-in-Memory Circuits III
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Shuenn-Yuh Lee (National Cheng Kung University)

ID1733: **Time-Based Sensing with Linear Current-to-Time Conversion for Multi-Level Resistive Memory**
Byungkwon An (Nanyang Technological University, Singapore), Xueyong Zhang (Nanyang Technological University, Singapore), Anh Tuan Do (Institute of Microelectronics, Agency for Science, Technology and Research, Singapore), Tony Tae-Hyoung Kim (Nanyang Technological University, Singapore)

ID1853: **NS-Engine: Near-Sensor Neural Network Engine with SRAM-Based Compute-in-Memory Macro**

Erxiang Ren (Beijing Jiaotong University, China), Jiahui Liu (Beijing Jiaotong University, China), Li Luo (Beijing Jiaotong University, China), Xinghua Yang (Beijing Forestry University, China), Qi Wei (Tsinghua University, China), Fei Qiao (Tsinghua University, China)

ID2187: SRAM-Based Digital CIM Macro for Linear Interpolation and MAC
Zhiting Lin (Anhui University, China), Yunlong Liu (Anhui University, China), Yaling Wang (Anhui University, China), Yue Zhao (Anhui University, China), Chunyu Peng (Anhui University, China), Xiulong Wu (Anhui University, China)

ID2437: MAC-DO: DRAM-Based Multi-Bit Analog Accelerator Using Output Stationary
Minki Jeong (Korea Advanced Institute of Science and Technology, Korea), Wanyeong Jung (Korea Advanced Institute of Science and Technology, Korea)

ID2491: A 0.5 μm² 2-T Thin-Oxide OTP Antifuse with Reliability Enhanced by Auto Shut-Off Program Logic for Low-Power Applications
Haoyu Li (Peking University, China), Dong Wang (Peking University, China), Jiazheng Zhou (Peking University, China), Junhua Liu (Peking University, China), Huailin Liao (Peking University, China)

3:00 pm – 5:00 pm
C5P-18 Circuits & Systems for Switch-Mode DC-DC Power Supplies
TRACK 4: POWER AND ENERGY CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Yanzhao Ma (Northwestern Polytechnical University)

ID2204: A Switched-Photovoltaic Ladder DC-DC Converter for High Harvesting Efficiency Under Nonuniform Illumination
Loai G. Salem (University of California, Santa Barbara, United States)

ID1439: A 60-Na IQ 96.5% Peak Efficiency Buck Converter with Wide Load Range for Internet of Things
Ruijie Xi (Zhejiang University, China), Chenkang Xue (Zhejiang University, China), Jiping Li (Beijing Smart-Chip Microelectronics Technology Co. Ltd., China), Tianting Zhao (Beijing Smart-Chip Microelectronics Technology Co. Ltd., China), Mengjiao Li (Beijing Smart-Chip Microelectronics Technology Co. Ltd., China), Yong Ding (Zhejiang University, China), Wuhua Li (Zhejiang University, China), Wanyuan Qu (Zhejiang University, China)

ID2337: Capacitor-Less Buck-Boost Converter Using Integrated Planar Inductor-Capacitor Fabricated with Nanotechnology Processes
Haitham Kanakri (Purdue University Indianapolis, United States), Euzeli Cipriano Dos Santos Jr. (Purdue University Indianapolis, United States), Maher Rizkalla (Purdue University Indianapolis, United States)

ID2422: A 24V-to-1V Hybrid Converter with Adaptive Dead Time Control for Point-of-Load Applications
Guozhen Chang (Hong Kong University of Science and Technology, China), Yang Liu (Hong Kong University of Science and Technology, China), Wing-Hung Ki (Hong Kong University of Science and Technology, Hong Kong)

ID2537: A High-Voltage Single-Inductor Multiple-Output DC-DC Buck Converter for the Power Management Unit of a Gate-Shaping Digital Gate Driver
Tobias Zekorn (RWTH Aachen University, Germany), Florian Schimkat (RWTH Aachen University, Germany), Kenny Vohl (RWTH Aachen University, Germany), Erik Wehr (RWTH Aachen University,

Germany), Ralf Wunderlich (RWTH Aachen University, Germany), Stefan Heinen (RWTH Aachen University, Germany)

3:00 pm – 5:00 pm
C5P-19 6G, IoT Systems & Sensor Networks II
TRACK 3: COMMUNICATIONS CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Dur-e-Shahwar Kundi (PQShield Ltd, UK), Yuan-Hao Huang (National Tsing Hua University)

ID1391: **Efficient Hardware Design of DNN for RF Signal Modulation Recognition**
Jongseok Woo (Georgia Institute of Technology, United States), Kuchul Jung (Georgia Institute of Technology, United States), Saibal Mukhopadhyay (Georgia Institute of Technology, United States)

ID1392: **Enhancing IoT Security with a Hardware Accelerated Machine Learning Model Coupling Autoencoder and Long-Short-Term-Memory for Anomaly Detection**
Kuchul Jung (Georgia Institute of Technology, United States), Jongseok Woo (Georgia Institute of Technology, United States), Saibal Mukhopadhyay (Georgia Institute of Technology, United States)

ID1612: **Hardware Acceleration of Phase and Gain Control for Analog Beamforming**
Xinhao Mao (Fudan University, China), Ziyu Guo (Fudan University, China), Jun Han (Fudan University, China), Bo Hu (Fudan University, China), Xiaoyang Zeng (Fudan University, China)

ID1291: **A Multi-Constraint and Multi-Objective Allocation Model for Emergency Rescue in IoT Environment**
Xinrun Xu (University of the Chinese Academy of Sciences, China), Zhanbiao Lian (University of the Chinese Academy of Sciences, China), Yurong Wu (University of the Chinese Academy of Sciences, China), Manying Lv (University of the Chinese Academy of Sciences, China), Zhiming Ding (Institute of Software Chinese Academy of Sciences, China), Jin Yan (University of Chinese Academy of Sciences, China), Shan Jiang (Advanced Institute of Big Data, China)

3:00 pm – 5:00 pm
C5P-20 Wireless & Implantable Biomedical Circuits & Systems
TRACK 6: BIOMEDICAL CIRCUITS AND SYSTEMS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Shuenn Yuh (National Cheng Kung University, Taiwan)

ID1435: **A Lossless Neural Recording SoC for Epilepsy Monitoring with Up to 84.9-dB Dynamic Range and Rail-to-Rail Stimulation Artifact Tolerance**
Yirui Liu (Fudan University, China), Yukun Ding (Fudan University, China), Xiao Liu (Fudan University, China)

ID1823: **On-Chip 5&6-GHz RF Energy Harvesting System for Implantable Medical Devices**
Pranay Kamal Miriyala (Indian Institute of Technology Dharwad, India), P Nitin Srinivas (Indian Institute of Technology Dharwad, India), Dr Nagaveni S (Indian Institute of Technology Dharwad, India)

ID1917: **A Lumped Circuit Model for Implantable Body-Coupled Channel**
Cheng Han (Institute of Automation, Chinese Academy of Sciences, China), Shan Yu (Institute of Automation, Chinese Academy of Sciences, China), Zhiwei Zhang (Institute of Automation, Chinese

Academy of Sciences, China), Jingna Mao (Institute of Automation, Chinese Academy of Sciences, China)

ID2355: **On the New Analytical Design of Efficient Inductive Links with Maximum Biomedical Wireless Power Transfer Capability and Area Controllability**
Asif Iftekhar Omi (University of Florida, United States), Baibhab Chatterjee (University of Florida, United States)

ID2586: **A Low-Power Level-Crossing Analog-to-Spike Converter Intended for Neuromorphic Biomedical Applications**
Jinbo Chen (Westlake University & Zhejiang University, China), Hui Wu (Westlake University, China), Fengshi Tian (Hong Kong University of Science and Technology, Hong Kong), Qiming Hou (Westlake University, China), Siyu Lin (Westlake University, China), Jie Yang (Westlake University, China), Mohamad Sawan (Westlake University, China)

3:00 pm – 5:00 pm
C5P-21 Neuromorphic Spiking Learning Systems & Applications III
TRACK 8: NEURAL NETWORKS AND NEUROMORPHIC ENGINEERING

Venue: Leo 2+3+4
POSTER
Session Chair(s): Qinyu Chen (Leiden University)

ID1619: **A Scalable and PVT Invariant Spiking Neuron Using Asynchronous CMOS Logic**
Dante Loi (Universidad Carlos III de Madrid, Spain), Javier Granizo (Universidad Carlos III de Madrid, Spain), Luis Hernandez (Universidad Carlos III de Madrid, Spain)

ID1812: **A 1024-Neuron 1M-Synapse Event-Driven SNN Accelerator for DVS Applications**
Xi Cheng (Fudan University, China), Shu Cao (Fudan University, China), Shangmei Wang (Fudan University, China), Xiaoyang Zeng (Fudan University, China), Wenhong Li (Fudan University, China), Mingyu Wang (Fudan University, China)

ID1817: **PEFSL: A Deployment Pipeline for Embedded Few-Shot Learning on a FPGA SoC**
Lucas Grativol Ribeiro (IMT Atlantique Bretagne-Pays de la Loire, Lab-STICC, France), Lubin Gauthier (IMT Atlantique Bretagne-Pays de la Loire, Lab-STICC, France), Mathieu Léonardon (IMT Atlantique Bretagne-Pays de la Loire, Lab-STICC, France), Jérémy Morlier (IMT Atlantique Bretagne-Pays de la Loire, Lab-STICC, France), Antoine Lavrard-Meyer (IMT Atlantique Bretagne-Pays de la Loire, Lab-STICC, France), Guillaume Muller (Mines Saint-Etienne, Institut Henri Fayol, France), Virginie Fresse (Hubert Curien Laboratory, France), Matthieu Arzel (IMT Atlantique Bretagne-Pays de la Loire, Lab-STICC, France)

ID1909: **Towards Fair and Firm Real-Time Scheduling in DNN Multi-Tenant Multi-Accelerator Systems via Reinforcement Learning**
Enrico Russo (Università degli studi di Catania, Italy), Francesco Blanco (Università degli studi di Catania, Italy), Maurizio Palesi (Università degli studi di Catania, Italy), Giuseppe Ascia (Università degli studi di Catania, Italy), Davide Patti (Università degli studi di Catania, Italy), Vincenzo Catania (Università degli studi di Catania, Italy)

ID1922: **Bayesian Inference Accelerator for Spiking Neural Networks**
Prabodh Katti (King's College London, United Kingdom), Anagha Nimbekar (Indian Institute of Technology Hyderabad, India), Chen Li (King's College London, United Kingdom), Amit Acharyya (Indian Institute of Technology Hyderabad, India), Bashir M. Al-Hashimi (King's College London, United Kingdom), Bipin Rajendran (King's College London, United Kingdom)

ID1626: [A Compact 140nW/Input Winner-Take-All Circuit for Spiking Neural Networks]
Gaurav R (Indian Institute of Technology Bombay, India), Abhishek A. Kadam (Indian Institute of Technology Bombay, India), Ajay K. Singh (Indian Institute of Technology Bombay, India), Laxmeesha Somappa (Indian Institute of Technology Bombay, India), Maryam Shojaei Baghini (Indian Institute of Technology Bombay, India), Udayan Ganguly (Indian Institute of Technology Bombay, India)

3:00 pm – 5:00 pm
C5P-22 Algorithms & Hardware for Low-complexity Visual Signal Processing
TRACK 11: VISUAL SIGNAL PROCESSING AND COMMUNICATIONS

Venue: Leo 2+3+4
POSTER
Session Chair(s): Ying Liu (Santa Clara University)

ID1084: [USR-LUT: A High-Efficient Universal Super Resolution Accelerator with Lookup Table]
Xin Zhao (University of Electronic Science and Technology of China, China), Zhicheng Hu (University of Electronic Science and Technology of China, China), Liang Chang (University of Electronic Science and Technology of China, China)

ID2259: [An Efficient Hardware Volume Renderer for Convolutional Neural Radiance Fields]
Xuexin Wang (ShanghaiTech University, China), Yunxiang He (ShanghaiTech University, China), Xiangyu Zhang (ShanghaiTech University, China), Pingqiang Zhou (ShanghaiTech University, China), Xin Lou (ShanghaiTech University, China)

ID2412: [An FPGA-Based Ultra-High Performance and Scalable Optical Flow Hardware Accelerator for Autonomous Driving]
Ye Liu (University of Electronic Science and Technology of China, China), Shuang Hao (University of Electronic Science and Technology of China, China), Kun Huang (University of Electronic Science and Technology of China, China), Minghui Yang (University of Electronic Science and Technology of China, China), Zili Huang (University of Electronic Science and Technology of China, China), Xiuyuan Qi (University of Electronic Science and Technology of China, China), Yiting Li (University of Electronic Science and Technology of China, China), Liang Zhou (University of Electronic Science and Technology of China, China), Yu Long (University of Electronic Science and Technology of China, China), Jun Zhou (University of Electronic Science and Technology of China, China)

ID2475: [A High-Performance ORB Accelerator with Algorithm and Hardware Co-Design for Visual Localization]
Xiuyuan Qi (University of Electronic Science and Technology of China, China), Ye Liu (University of Electronic Science and Technology of China, China), Shuang Hao (University of Electronic Science and Technology of China, China), Zherong Liu (University of Electronic Science and Technology of China, China), Kun Huang (University of Electronic Science and Technology of China, China), Minghui Yang (University of Electronic Science and Technology of China, China), Liang Zhou (University of Electronic Science and Technology of China, China), Jun Zhou (University of Electronic Science and Technology of China, China)

ID1765: [Redundancy Removal Module for Reducing the Bitrates of Image Coding for Machines]
Zhongpeng Zhang (Santa Clara University, United States), Ying Liu (Santa Clara University, United States)

ID2244: [Robust DNA Image Storage Decoding with Residual CNN]

Cihan Ruan (Santa Clara University, United States), Liang Yang (Nankai University, China), Rongduo Han (Nankai University, China), Shan Gao (Nankai University, China), Haoyu Wu (Roku Inc., United States), Nam Ling (Santa Clara University, United States)

3:00 pm – 5:00 pm
C5P-23 Neural Learning Systems: Transformers & Applications II
TRACK 8: NEURAL NETWORKS AND NEUROMORPHIC ENGINEERING

Venue: Leo 2+3+4
POSTER
Session Chair(s): Shih-Chii Liu (University of Zurich - ETH Zürich)

ID1309: **Swin Transformer for Pedestrian and Occluded Pedestrian Detection**
Jung-An Liang (National Taiwan University, Taiwan), Jian-Jiun Ding (National Taiwan University, Taiwan)

ID1515: **Axial Attention Transformer for Fast High-Quality Image Style Transfer**
Yuxin Liu (Southwest University of Science and Technology, China), Wenxin Yu (Southwest University of Science and Technology, China), Zhiqiang Zhang (Southwest University of Science and Technology, China), Qi Wang (Southwest University of Science and Technology, China), Lu Che (Southwest University of Science and Technology, China)

ID1645: **Spiking-Hybrid-YOLO for Low-Latency Object Detection**
Mingxin Guo (Institute of Automation, Chinese Academy of Sciences, China), Dongjun Xu (Institute of Automation, Chinese Academy of Sciences, China), Yaoyao Li (Institute of Automation, Chinese Academy of Sciences, China), Jian Cheng (Institute of Automation, Chinese Academy of Sciences, China), Liang Chen (Institute of Automation, Chinese Academy of Sciences, China)

ID1975: **DehazeDiff: When Conditional Guidance Meets Diffusion Models for Image Dehazing**
Longyu Cheng (Xiamen University, China), Xujin Ba (Shanghai Jiao Tong University, China), Yanyun Qu (Xiamen University, China)

ID2125: **A Memory-Efficient High-Speed Event-Based Object Tracking System**
Yuncheng Lu (Nanyang Technological University, Singapore), Kaixiang Cui (Nanyang Technological University, Singapore), Yucen Shi (Nanyang Technological University, Singapore), Zehao Li (Nanyang Technological University, Singapore), Junying Li (Nanyang Technological University, Singapore), Wenhao Lu (Nanyang Technological University, Singapore), Yuanjin Zheng (Nanyang Technological University, Singapore), Tony Tae-Hyoung Kim (Nanyang Technological University, Singapore)

ID2226: **CNN Model with Transfer Learning and Data Augmentation for Obstacle Detection in Rail Systems**
Hocine Kaddour Drizi (Université du Québec à Montréal, Canada), Mounir Boukadoum (Université du Québec à Montréal, Canada)

3:30 pm – 5:00 pm
C6L-01 Analog Techniques II
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Aquarius 1
ORAL
Session Chair(s): Edoardo Bonizzoni (University of Pavia), Yuxuan Luo (Zhejiang University)

3:30 pm
ID1841: **A Non-Trimmed, 7 MHz and 52 ppm/℃ Relaxation Oscillator with Loop Errors Compensation from -40℃ to 165℃**
Jianlin Xia (Southeast University, China), Yongjia Li (Southeast University, China), Zhongyuan Fang (Southeast University, China), Jin Wu (Southeast University, China), Feng Lin (Central Semiconductor Manufacturing Corporation, China), Weifeng Sun (Southeast University, China)

3:48 pm
ID1879: **A DEM Structure Based on Random Combination Group Encoding Toward a Reduced Circuit Area**
Yujie Xian (University of Electronic Science and Technology of China, China), Jiyi Liu (University of Electronic Science and Technology of China, China), Shang Ma (University of Electronic Science and Technology of China, China), Bowen Li (University of Electronic Science and Technology of China, China), Runsen Yan (University of Electronic Science and Technology of China, China), Mengtao Yang (University of Electronic Science and Technology of China, China)

4:06 pm
ID1678: **A 2^7-1, 20-Gb/s, 0.1-pJ/b Pseudo Random Bit Sequence Generator Using Incomplete Settling in 1.2V, 65 nm CMOS**
Prema Kumar Govindaswamy (Indian Institute of Technology Bhubaneswar, India), Mursina Khatun (Indian Institute of Technology Bhubaneswar, India), Vijay Shankar Pasupureddi (Indian Institute of Technology Bhubaneswar, India)

4:24 pm
ID2321: **A One-Point-Trimmed 18.4 ppm/℃ On-Chip Oscillator with Capacitively-Biased-Diode-Based Quasi-Digital Temperature Compensation**
Yonghong Kuang (Zhejiang University, China), Yekan Chen (Zhejiang University, China), Tianyi Cai (Zhejiang University, China), Qi Zhang (Zhejiang University, China), Zipeng Cheng (Zhejiang University, China), Bo Zhao (Zhejiang University, China), Yuxuan Luo (Zhejiang University, China)

4:42 pm
ID2376: **An Automatic PCB Imposition Method Based on Reinforcement Learning**
Zhaoting Ou (University of Electronic Science and Technology of China, China), Jienan Chen (University of Electronic Science and Technology of China, China), Jie Zheng (University of Electronic Science and Technology of China, China)

3:30 pm – 5:00 pm
C6L-02 Time Interleaved & SAR ADC
TRACK 1: ANALOG AND MIXED SIGNAL CIRCUITS AND SYSTEMS

Venue: Aquarius 2
ORAL
Session Chair(s): Qiang Li (University of Electronic Science and Technol), Shahriar Mirabbasi (University of British Columbia)

3:30 pm
ID1213: **Analysis of Random Clock Jitter Effect in Time-Interleaved DACs**
Hong Chen (Zhejiang University, China), Nan Wang (Zhejiang University, China), Xiang Gao (Zhejiang University, China)

3:48 pm
ID2058: **On the Application of Data Weighted Averaging to Noise Shaping SAR ADCs**

David Rivera-Orozco (Microelectronic Circuits Centre Ireland / CINVESTAV-Guadalajara Unit, Ireland), Federico Sandoval-Ibarra (CINVESTAV Guadalajara, Mexico), Gerardo Molina Salgado (Microelectronic Circuits Centre Ireland, University College Cork, Ireland)

4:06 pm
ID2332: **An 800 kS/s 1.83 fJ/conv. 12b ADC via Voltage Successive Approximation and Gated Cyclic Vernier Time Digitization**
Ian Perczak (Toronto Metropolitan University, Canada), Fei Yuan (Toronto Metropolitan University, Canada)

4:24 pm
ID2400: **Enhancing Performance of SAR ADC Through Supervised Machine Learning**
Sumukh Bhanushali (Arizona State University, United States), Arindam Sanyal (Arizona State University, United States)

4:42 pm
ID1741: **An 11-Bit 12 GS/s Beam-Forming Receiver ADC for a 2x2 Antenna Array Utilizing True Time-Delay with 68 dBc SFDR and 55 dB SNDR**
Enne Wittenhagen (Technische Universität Berlin, Germany), Dominik Wilding (Technische Universität Berlin, Germany), Patrick Kurth (Technische Universität Berlin, Germany), Sebastian Linnhoff (Technische Universität Berlin, Germany), Frowin Buballa (Technische Universität Berlin, Germany), Urs Hecht (Technische Universität Berlin, Germany), Patrick Artz (Technische Universität Berlin, Germany), Friedel Gerfers (Technische Universität Berlin, Germany)

3:30 pm – 5:00 pm
C6L-03 Hardware Security for Logic, Circuits & Architectures II
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Aquarius 3
ORAL
Session Chair(s): Yue Zheng (Chinese University of Hong Kong), Preet Yadav (NXP Semiconductors, India)

3:30 pm
ID1832: **DNA: DC Nodal Analysis Attack for Analog Circuits**
Vaibhav Venugopal Rao (Drexel University, United States), Kyle Juretus (Villanova University, United States), Ioannis Savidis (Drexel University, United States)

3:48 pm
ID2057: **Area-Efficient Matrix-Vector Polynomial Multiplication Architecture for ML-KEM Using Interleaving and Folding Transformation**
Weihang Tan (University of Minnesota, United States), Yingjie Lao (Tufts University, United States), Keshab K. Parhi (University of Minnesota, United States)

4:06 pm
ID1982: **In-Memory Encryption Using XOR-Based Feistel Cipher in SRAM Array**
Kavitha Soundrapandiyan (Indian Institute of Information Technology, Design and Manufacturing, Kancheepuram, India), Bhupendra Singh Reniwal (Indian Institute of Technology Jodhpur, India)

4:24 pm
ID1564: **HWSim: Hardware Similarity Learning for Intellectual Property Piracy Detection**
Zirui Jiang (University of the Chinese Academy of Sciences, China), Xiao Ji (University of the Chinese Academy of Sciences, China), Yiran He (University of the Chinese Academy of Sciences, China), Haihua Shen (University of Chinese Academy of Sciences, China)

4:42 pm
ID1369: **A Fault Attack Resistant Method for RISC-V Based on Interrupt Handlers and Instruction Extensions**
Jiashuo Wei (Tianjin University, China), Qiang Liu (Tianjin University, China)

3:30 pm – 5:00 pm
C6L-04 Electronic Design Automation & Physical Design I
TRACK 2: DIGITAL INTEGRATED CIRCUITS AND SYSTEMS

Venue: Aquarius 4
ORAL
Session Chair(s): Ioannis Savidis (Drexel University), Yuhang Zhang (Shanghai Jiao Tong University)

3:30 pm
ID2190: **Tetris-SDK: Efficient Convolution Layer Mapping with Adaptive Windows for Fast in Memory Computing**
Ke Dong (Singapore University of Technology and Design, Singapore), Kejie Huang (Zhejiang University, China), Bo Wang (Singapore University of Technology and Design, Singapore)

3:48 pm
ID1249: **SERS-3DPlace: Ensemble Reinforcement Learning for 3D Monolithic Placement**
Abdullah Mansoor (Portland State University, United States), Malgorzata Chrzanowska-Jeske (Portland State University, United States)

4:06 pm
ID2499: **Instance-Level Timing Learning and Prediction at Placement Using Res-UNet Network**
He Liu (Peking University, Peng Cheng Laboratory, China), Simin Tao (Peng Cheng Laboratory, China), Zhipeng Huang (Peng Cheng Laboratory, China), Biwei Xie (Institute of Computing Technology, Chinese Academy of Sciences, Peng Cheng Laboratory, China), Xingquan Li (Minnan Normal University, Peng Cheng Laboratory, China), Ge Li (Peking University, China)

4:24 pm
ID1664: **An Enhanced Resubstitution Algorithm for Area-Oriented Logic Optimization**
Andrea Costamagna (École Polytechnique Fédérale de Lausanne, Switzerland), Alan Mishchenko (University of California, Berkeley, United States), Satrajit Chatterjee (Kepler AI, United States), Giovanni De Micheli (École Polytechnique Fédérale de Lausanne, Switzerland)

4:42 pm
ID2311: **ANN-Based Accurate and Fast Post-Route QoR Data Prediction Methodology from Pre-Clock Tree Synthesis by Skipping CTS and Routing**
Arpit Jain (Indian Institute of Technology Hyderabad, India), Pabitra Das (Indian Institute of Technology Hyderabad, India), Amit Acharyya (Indian Institute of Technology Hyderabad, India), Rakesh M B (Indian Institute of Technology Hyderabad, India)

3:30 pm – 5:00 pm
C6L-05 Computing with Emergent Technologies I
TRACK 5: BEYOND CMOS: NANOELECTRONICS AND HYBRID SYSTEMS INTEGRATION

Venue: Gemini 1
ORAL

Session Chair(s): Georgios Sirakoulis (Democritus University of Thrace), Vita Pi-Ho Hu (National Taiwan University)

3:30 pm
ID2189: **Complementary Series-Connected STT-MTJ for Time-Based Computing-in-Memory**
Rong Zhou (Southeast University, China), Bo Liu (Southeast University, China), Xin Si (Southeast University, China), Hao Cai (Southeast University, China)

3:48 pm
ID1800: **Device Codesign Using Reinforcement Learning**
Suma Cardwell (Sandia National Laboratories, United States), Karan Patel (University of Tennessee, United States), Catherine Schuman (University of Tennessee, United States), J. Darby Smith (Sandia National Laboratories, United States), Jaesuk Kwon (University of Texas at Austin, United States), Andrew Maicke (University of Texas at Austin, United States), Jared Arzate (University of Texas at Austin, United States), Jean Anne Incorvia (University of Texas at Austin, United States)

4:06 pm
ID1133: **Nonvolatile and SEU-Recoverable Latch Based on FeFET and CMOS for Energy-Harvesting Devices**
Aibin Yan (Anhui University & Hefei University of Technology, China), Zhuoyuan Lin (Anhui University, China), Guangzhu Liu (Hefei University of Technology, China), Qingyang Zhang (Anhui University, China), Zhengfeng Huang (Hefei University of Technology, China), Jie Cui (Anhui University, China), Xiaoqing Wen (Kyushu Institute of Technology, Japan), Patrick Girard (University of Montepllier, France)

4:24 pm
ID1842: **SAR-MemPipe: A Hybrid Pipeline-SAR Memristive ADC for Analog Resistive Arrays**
Hao You (University of Toronto, Canada), Jianxong Xu (University of Toronto, Canada), Amirali Amirsoleimani (York University, Canada), Mostafa Rahimi Azghadi (James Cook University, Australia), Roman Genov (University of Toronto, Canada)

4:42 pm
ID1819: **An Energy-Efficient Graphene-Based Spiking Neural Network Architecture for Pattern Recognition**
Nicoleta Cucu Laurenciu (Radboud University, Netherlands), Charles Timmermans (Radboud University, Netherlands), Sorin D. Cotofana (Delft University of Technology, Netherlands)

3:30 pm – 5:00 pm
C6L-06 2D/3D Image Sensors
TRACK 7: SENSORY CIRCUITS AND SYSTEMS

Venue: Gemini 2
ORAL
Session Chair(s): Shoushun Chen (Nanyang Technological University, Singapore), Amine Bermak (Hamad Bin Khalifa University, Doha, Qatar)

3:30 pm
ID1433: **An Indirect Time-of-Flight Sensor with Adaptive Multiple Sampling for High Depth Precision**
Jung-Hye Hwang (Ulsan National Institute of Science and Technology, Korea), Jubin Kang (Ulsan National Institute of Science and Technology, Korea), Yongjae Park (Ulsan National Institute of Science and Technology, Korea), Insang Son (Ulsan National Institute of Science and Technology, Korea), Kieop Hong (Ulsan National Institute of Science and Technology, Korea), Seong-Jin Kim (Ulsan National Institute of Science and Technology, Korea)

3:48 pm
ID2229: **A Novel Balanced Detection Based Optoelectronic Front End Circuit for FMCW LiDAR System**
Wenming Zhu (Huazhong University of Science and Technology, China), Weitao Yuan (Huazhong University of Science and Technology, China), Dan Wu (Huazhong University of Science and Technology, China), Yuansheng Zhao (Huazhong University of Science and Technology, China), Zhenghao Lu (Soochow University, China), Guoyi Yu (Huazhong University of Science and Technology, China), Yu Yu (Huazhong University of Science and Technology, China), Chao Wang (Huazhong University of Science and Technology, China)

4:06 pm
ID1555: **A Low-Power Multimode Eight-Channel AFE for dToF LiDAR**
Yuye Yang (Xi'an Jiaotong University, China), Xi Liu (Xi'an Jiaotong University, China), Ruixuan Yang (Xi'an Jiaotong University, China), Shuaizhe Ma (Xi'an Jiaotong University, China), Yifei Xia (Xi'an Jiaotong University, China), Jia Li (Xi'an Jiaotong University, China), Bing Zhang (Xi'an Jiaotong University, China), Li Geng (Xi'an Jiaotong University, China), Dan Li (Xi'an Jiaotong University, China)

4:24 pm
ID1075: **A 128×128 CMOS SPAD Receiver for 500Mbps Free Space Optical Communication with Column-Wise Decoding and Fast Spot Tracking**
Bu Chen (Fudan University, China), Zhangcheng Huang (Fudan University, China), Qi Liu (Fudan University, China)

4:42 pm
ID2142: **Low-Noise Image Sensors with Shifted Pseudo-Correlated Multiple Sampling Method**
Su Yeon Yun (Dongguk University, Korea), Minkyu Song (Dongguk University, Korea), Soo Youn Kim (Dongguk University, Korea)

3:30 pm – 5:00 pm
C6L-07 Lab-on-Chip & Point-of-Care Biomedical Diagnostics
TRACK 6: BIOMEDICAL CIRCUITS AND SYSTEMS

Venue: Pisces 1
ORAL
Session Chair(s): Sohmyung Ha (New York Univeristy), Matthew Johnston (Oregon State University, USA)

3:30 pm
ID1183: **A Programmable CMOS Dielectrophoresis Array Chip with 128×128 Electrodes for Cell Manipulation**
Wen-Yue Lin (National Yang Ming Chiao Tung University, Taiwan), Lin-Hung Lai (National Yang Ming Chiao Tung University, Taiwan), Yi-Wei Lin (National Yang Ming Chiao Tung University, Taiwan), Chen-Yi Lee (National Yang Ming Chiao Tung University, Taiwan)

3:48 pm
ID1190: **A Microfluidic Impedance Cytometer for Accurate Detection and Counting of Circulating Tumor Cells by Simultaneous Mechanical and Electrical Sensing**
Xiang Ke (Hangzhou Dianzi University, China), Jin Chen (Hangzhou Dianzi University, China), Jingjing Sun (Hangzhou Dianzi University, China), Rikui Xiang (Hangzhou Dianzi University, China), Wenjing Fang (Hangzhou Dianzi University, China), Liangzun Fu (Hangzhou Dianzi University, China), Xiwei Huang (Hangzhou Dianzi University, China), Yan Xia (Zhejiang University, China),

Jinhong Guo (Shanghai Jiao Tong University, China), Lingling Sun (Hangzhou Dianzi University, China)

4:06 pm
ID1480: **A Highly Parallel Capacitive Sensing Circuit for High-Throughput Thin-Film Transistor Digital Microfluidic Chips**
Lingxiao Qian (Peking University, China), Congwei Liao (Peking University, China), Yuhan Zhang (Peking University, China), Yong Le (Peking University, China), Shengdong Zhang (Peking University, China)

4:24 pm
ID2369: **A 174.8 dB FoMs CT-ΔΣ ADC with Integrated ISFET Sensor and Noise-Shaping Enhancement**
Chen Wang (Beihang University, China), Yuanqi Hu (Beihang University, China)

4:42 pm
ID2324: **A Low Power Analogue Compressed Sensing Approach for CMOS ISFET Arrays**
Shuanghua Liu (Imperial College London, United Kingdom), Junming Zeng (Imperial College London, United Kingdom), Pantelis Georgiou (Imperial College London, United Kingdom)

3:30 pm – 5:00 pm
C6L-09 Biomedical Signal & Image Processing
TRACK 10: DIGITAL SIGNAL PROCESSING

Venue: Pisces 3
ORAL
Session Chair(s): Izzet Kale (University of Westminster, UK), Jiuwen Cao(Hangzhou Dianzi University, China)
Track: 10

3:30 pm
ID1068: **Automatic EEG-Based Spike Ripples Detection with Multi-Band Frequency Analysis**
Sihan Zhou (Hangzhou Dianzi University, China), Dinghan Hu (Hangzhou Dianzi University, China), Feng Gao (Zhejiang University School of Medicine, China), Tiejia Jiang (Zhejiang University School of Medicine, China), Jiuwen Cao (Hangzhou Dianzi University, China)

15:48 pm
ID1331: **RecogNoise: Machine-Learning-Based Recognition of Noisy Segments in Electrocardiogram Signals**
Amin Aminifar (Heidelberg University, Germany), Soheil Khooyooz (Heidelberg University, Germany), Anice Jahanjoo (Technische Universität Wien, Austria), Salar Shakibhamedan (Technische Universität Wien, Austria), Nima TaheriNejad (Heidelberg University, Germany)

4:06 pm
ID1462: **Optimal Filtering and Smoothing Thresholds for High-Frequency Photoplethysmography Signals**
Stefan Karolcik (Imperial College London, United Kingdom), Pantelis Georgiou (Imperial College London, United Kingdom)

4:24 pm
ID2348: **MAGNet: A Convolutional Neural Network with Multi-Scale and Global Attention Modules for Medical Image Segmentation**
Subrato Bharati (Concordia University, Canada), M. Omair Ahmad (Concordia University, Canada), M.N.S. Swamy (Concordia University, Canada)

3:30 pm – 5:00 pm
C6L-10 Intelligent & Data Analytics to Real-Life Complex Networks & Nonlinear Systems II
TRACK 14: SPECIAL SESSION

Venue: Pisces 4
ORAL
Session Chair(s): Xi Zhang (Beijing Institute of Technology), Yongxiang Xia (Hangzhou Dianzi University)

3:30 pm
ID2318: Cooperative Emergence in Structured Populations Mixed with Imitation and Aspiration Learning Dynamics
Zhizhuo Zhou (Donghua University, China), Jing Zhang (Donghua University, China), Zhihai Rong (Donghua University, China)

3:48 pm
ID2416: Strengthening Critical Power Network Branches for Cascading Failure Mitigation
Biwei Li (City University of Hong Kong, Hong Kong), Dong Liu (City University of Hong Kong, Hong Kong), Junyuan Fang (City University of Hong Kong, Hong Kong), Xi Zhang (Beijing Institute of Technology, China), Chi Kong Tse (City University of Hong Kong, Hong Kong)

4:06 pm
ID2432: Analysis of Reservoir Computing Using Oscillator Circuit
Kazuki Yasufuku (Tokushima University, Japan), Yoko Uwate (Tokushima University, Japan), Yoshifumi Nishio (Tokushima University, Japan)

4:24 pm
ID1271: Fault Detection and Location of Transmission Lines Based on Convolutional Neural Network
Yangyang Jiang (Hangzhou Dianzi University, China), Chang Sun (Hangzhou Dianzi University, China), Yongxiang Xia (Hangzhou Dianzi University, China), Haicheng Tu (Hangzhou Dianzi University, China), Chunshan Liu (Hangzhou Dianzi University, China)

4:42 pm
ID2250: Longitudinal Control for Mixed Vehicle Platoon Using Mixed Spacing Policy
Boyu Liu (Chongqing University of Posts and Telecommunications, China), Yongfu Li (Chongqing University of Posts and Telecommunications, China), Longwang Huang (Chongqing University of Posts and Telecommunications, China)

3:30 pm – 5:00 pm
C6L-11 Millimeter-Wave & Sub-THz 5G/6G/SATCOM Broadband Circuits & Systems
TRACK 14: SPECIAL SESSION

Venue: Virgo 1
ORAL
Session Chair(s): Donald Lie (Texas Tech University), Chien-nan Kuo (National Yangming Chiao-Tung University)

3:30 pm
ID2140: Sub-THz CMOS Phased-Array Transceiver Design for 6G
Kenichi Okada (Tokyo Institute of Technology, Japan)

3:48 pm
ID2122: **Broadband High-Efficiency Watt-Level Millimeter-Wave GaN Power Amplifier for Potential Robust and Cost-Effective 5G RF Front-End Design**
Clint Sweeney (Texas Tech University, United States), Donald Lie (Texas Tech University, United States), Jill Mayeda (Texas Tech University, United States), Jerry Lopez (Noisefigure Research Inc and Texas Tech University, United States)

4:06 pm
ID1661: **A 24–71-GHz Tri-Mode Mixer Using Harmonic Selection for Multi-Band 5G NR**
Dongfan Xu (Tokyo Institute of Technology, Japan), Minzhe Tang (Tokyo Institute of Technology, Japan), Yi Zhang (Tokyo Institute of Technology, Japan), Zheng Li (Tokyo Institute of Technology, Japan), Atsushi Shirane (Tokyo Institute of Technology, Japan), Kenichi Okada (Tokyo Institute of Technology, Japan)

4:24 pm
ID1735: **A 70-to-110 GHz 28-nm CMOS Low Noise Amplifier with 6.1-dB NF Minimum Using Differential Noise Optimization**
Yung Pei Li (National Taiwan University, Taiwan), Wei-Ting Bai (National Taiwan University, Taiwan), Tian-Wei Huang (National Taiwan University, Taiwan), Chen Chien (ACADEMIA SINICA Institute of Astronomy and Astrophysics, Taiwan), Yuh-Jing Hwang (ACADEMIA SINICA Institute of Astronomy and Astrophysics, Taiwan)

4:42 pm
ID2123: **A Ka- to W-Band Tightly Coupled Array Antenna-in-Package Using Glass IPD for Ultrawideband mmWave Wireless Communication**
Ching-Wen Chiang (National Yang Ming Chiao Tung University, Taiwan), Neda Khiabani (Rutgers University, United States), Donglin Gao (Rutgers University, United States), Chien-Nan Kuo (National Yang Ming Chiao Tung University, Taiwan), Yen-Cheng Kuan (National Yang Ming Chiao Tung University, Taiwan), Chung-Tse Michael Wu (Rutgers University, United States)

5:00 pm – 6:00 pm
Conference Awards & ISCAS 2025 Presentation
SPECIAL EVENT

Venue: Leo 1
Session Chair(s): Amara Amara (Beihang University, China), Bah Hwee Gwee (Nanyang Technological University, Singapore)

6:00 pm – 9:00 pm
Farewell Reception
SOCIAL EVENT

Venue: Malaysian Food Street at Resorts World Sentosa

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